

Apéndice 3

Especificaciones de componentes.

MOSFET IRF840

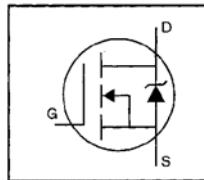
**International
IR Rectifier**

PD-9.376H

IRF840

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements

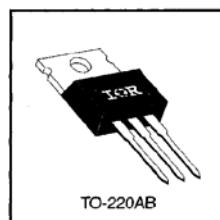


$V_{DSS} = 500V$
 $R_{DS(on)} = 0.85\Omega$
 $I_D = 8.0A$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	8.0	
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	5.1	A
I_{DM}	Pulsed Drain Current ①	32	
$P_D @ T_C = 25^\circ C$	Power Dissipation	125	W
	Linear Derating Factor	1.0	W/ $^\circ C$
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	510	mJ
I_{AR}	Avalanche Current ①	8.0	A
E_{AR}	Repetitive Avalanche Energy ①	13	mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.5	V/ns
T_J	Operating Junction and Storage Temperature Range	-55 to +150	$^\circ C$
T_{STG}	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf-in (1.1 N·m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
R_{JC}	Junction-to-Case	—	—	1.0	
R_{CS}	Case-to-Sink, Flat, Greased Surface	—	0.50	—	$^\circ C/W$
R_{JA}	Junction-to-Ambient	—	—	62	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(\text{BR})DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS}=0V, I_D=250\mu\text{A}$
$\Delta V_{(\text{BR})DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.78	—	V°C	Reference to 25°C , $I_D=1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.85	Ω	$V_{GS}=10V, I_D=4.8\text{A}$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$
g_f	Forward Transconductance	4.9	—	—	S	$V_{DS}=50V, I_D=4.8\text{A}$ ④
$I_{DS(on)}$	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS}=500V, V_{GS}=0V$
		—	—	250		$V_{DS}=400V, V_{GS}=0V, T_J=125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS}=20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS}=-20V$
Q_g	Total Gate Charge	—	—	63	nC	$I_D=8.0\text{A}$
Q_{gs}	Gate-to-Source Charge	—	—	9.3		$V_{DS}=400V$
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	32		$V_{GS}=10V$ See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	14	—		$V_{DD}=250V$
t_r	Rise Time	—	23	—		$I_D=8.0\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	49	—		$R_G=9.1\Omega$
t_f	Fall Time	—	20	—		$R_D=31\Omega$ See Figure 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1300	—	pF	$V_{GS}=0V$
C_{oss}	Output Capacitance	—	310	—		$V_{DS}=25V$
C_{rss}	Reverse Transfer Capacitance	—	120	—		$f=1.0\text{MHz}$ See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	8.0	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	32		
V_{SD}	Diode Forward Voltage	—	—	2.0	V	$T_J=25^\circ\text{C}, I_S=8.0\text{A}, V_{GS}=0V$ ④
t_{rr}	Reverse Recovery Time	—	460	970	ns	$T_J=25^\circ\text{C}, I_F=8.0\text{A}$
Q_{rr}	Reverse Recovery Charge	—	4.2	8.9	μC	$dI/dt=100\text{A}/\mu\text{s}$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

③ $I_{SP}\leq 8.0\text{A}$, $dI/dt\leq 100\text{A}/\mu\text{s}$, $V_{DD}\leq V_{(\text{BR})DSS}$, $T_J\leq 150^\circ\text{C}$

② $V_{DD}=50V$, starting $T_J=25^\circ\text{C}$, $L=14\text{mH}$, $R_G=25\Omega$, $I_A=8.0\text{A}$ (See Figure 12)

④ Pulse width $\leq 300 \mu\text{s}$; duty cycle $\leq 2\%$.

OPTOACOPLADOR HCPL-4502



July 2005

Single-channel: 6N135, 6N136, HCPL-2503, HCPL-4502

Dual-Channel: HCPL-2530, HCPL-2531

High Speed Transistor Optocouplers

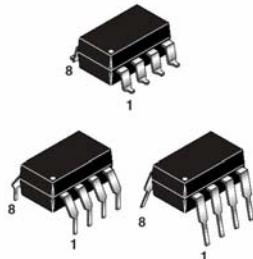
Features

- High speed-1 MBit/s
- Superior CMR-10 kV/μs
- Dual-Channel HCPL-2530/HCPL-2531
- Double working voltage-480V RMS
- CTR guaranteed 0-70%
- U.L. recognized (File # E90700)

Applications

- Line receivers
- Pulse transformer replacement
- Output interface to CMOS-LSTTL-TTL
- Wide bandwidth analog coupling

Package



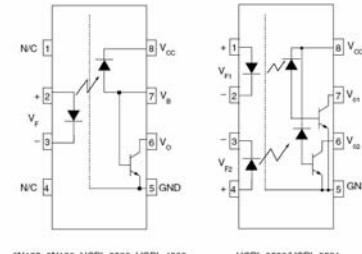
Description

The HCPL-4502/HCPL-2503, 6N135/6 and HCPL-2530/HCPL-2531 optocouplers consist of an AlGaAs LED optically coupled to a high speed photodetector transistor.

A separate connection for the bias of the photodiode improves the speed by several orders of magnitude over conventional phototransistor optocouplers by reducing the base-collector capacitance of the input transistor.

An internal noise shield provides superior common mode rejection of 10kV/μs. An improved package allows superior insulation permitting a 480 V working voltage compared to industry standard of 220 V.

Schematic



6N135, 6N136, HCPL-2503, HCPL-4502

Pin 7 is not connected in Part Number HCPL-4502

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Units
Storage Temperature	T_{STG}	-55 to +125	°C
Operating Temperature	T_{OPR}	-55 to +100	°C
Lead Solder Temperature	T_{SOL}	260 for 10 sec	°C
EMITTER			
DC/Average Forward Input Current	I_F (avg)	25	mA
Peak Forward Input Current (50% duty cycle, 1 ms P.W.)	I_F (pk)	50	mA
Peak Transient Input Current - ($\leq 1 \mu\text{s}$ P.W., 300 pps)	I_F (trans)	1.0	A
Reverse Input Voltage	V_R	5	V
Input Power Dissipation (6N135/6N136 and HCPL-2503/4502) (HCPL-2530/2531) Each Channel (Note 3)	P_D	100 45	mW
DETECTOR			
Average Output Current	I_O (avg)	8	mA
Peak Output Current	I_O (pk)	16	mA
Emitter-Base Reverse Voltage (6N135, 6N136 and HCPL-2503 only)	V_{EBR}	5	V
Supply Voltage	V_{CC}	-0.5 to 30	V
Output Voltage	V_O	-0.5 to 20	V
Base Current (6N135, 6N136 and HCPL-2503 only)	I_B	5	mA
Output power dissipation (6N135, 6N136, HCPL-2503, HCPL-4502) (Note 4) (HCPL-2530, HCPL-2531) Each Channel	P_D	100 35	mW

DRIVER IR4427

International
IR Rectifier

Data Sheet No. PD60177 Rev. E
IR4426/IR4427/IR4428(S) & (PbF)

DUAL LOW SIDE DRIVER

Features

- Gate drive supply range from 6 to 20V
- CMOS Schmitt-triggered inputs
- Matched propagation delay for both channels
- Outputs out of phase with inputs (IR4426)
- Outputs in phase with inputs (IR4427)
- OutputA out of phase with inputA and OutputB in phase with inputB (IR4428)
- Also available LEAD-FREE

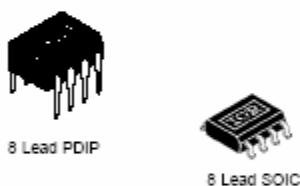
Descriptions

The IR4426/IR4427/IR4428 (S) is a low voltage, high speed power MOSFET and IGBT driver. Proprietary latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LS-TTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays between two channels are matched.

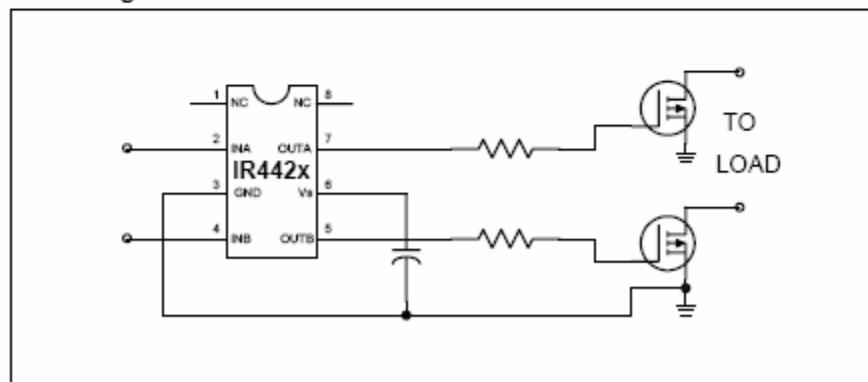
Product Summary

I _O +-	1.5A / 1.5A
V _{OUT}	6V - 20V
t _{on/off} (typ.)	85 & 65 ns

Packages



Block Diagram



IR4426/IR4427/IR4428(S) & (PbF)
ADVANCE INFORMATION

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Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_S	Fixed supply voltage	-0.3	25	V
V_O	Output voltage	-0.3	$V_S + 0.3$	
V_{IN}	Logic Input voltage	-0.3	$V_S + 0.3$	
P_O	Package power dissipation @ $T_A \leq 25^\circ\text{C}$	—	1.0	W
	(8 lead PDIP) (8 lead SOIC)	—	0.625	
R_{thJA}	Thermal resistance, junction to ambient	—	125	°C/W
	(8 lead PDIP) (8 lead SOIC)	—	200	
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to GND.

Symbol	Definition	Min.	Max.	Units
V_S	Fixed supply voltage	6	20	V
V_O	Output voltage	0	V_S	
V_{IN}	Logic input voltage	0	V_S	
T_A	Ambient temperature	-40	125	°C

DC Electrical Characteristics

V_{IN} (V_S) = 15V, T_A = 25°C unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to GND and are applicable to input leads: INA and INB. The V_O and I_O parameters are referenced to GND and are applicable to the output leads: OUTA and OUTB.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "0" Input voltage (OUTA=LO, OUTB=LO) (IR4426) Logic "1" Input voltage (OUTA=HI, OUTB=HI) (IR4427) Logic "0" Input voltage (OUTA=LO), Logic "1" Input voltage (OUTB=HI) (IR4428)	2.7	—	—	V	