Apéndice A

Hoja de datos técnicos MTP3055V

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Order this document
by MTP3055V/D

Designer's™ Data Sheet
TMOS V™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

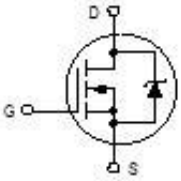
MTP3055V
Motorola Preferred Device

TMOS POWER FET
12 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.15 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

New Features of TMOS V
- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETS
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET



CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	60	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \leq 10$ ms)	V_{GS} V_{GSM}	± 20 ± 25	Vdc Vpk
Drain Current — Continuous @ 25°C — Continuous @ 100°C — Single Pulse ($t_p \leq 10$ µs)	I_D I_D I_{DM}	12 7.3 37	Adc Apk
Total Power Dissipation @ 25°C Derate above 25°C	P_D	48 0.32	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, I_L = 12 Apk, L = 1.0 mH, R_G = 25 Ω)	E_{AS}	72	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	3.13 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

E–FET, Designer's and TMOS V are trademarks of Motorola, Inc. TMOS is a registered trademark of Motorola, Inc.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

MOTOROLA