International
IOR Rectifier

Preliminary Data Sheet No. PD60166-O

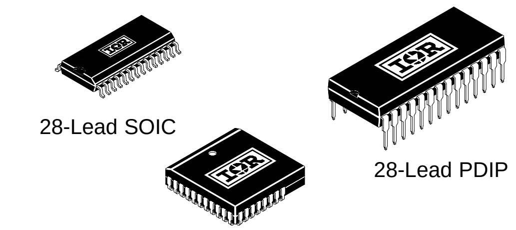
IR2136/IR21362/ IR21363/IR21365 (J&S)

3-PHASE BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V (IR2136), 11.5 to 20V (IR21362) or 12 to 20V (IR21363/IR21365)
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent 3 half-bridge drivers
- Matched propagation delay for all channels
- Lowside outputs out of phase with inputs. High side outputs out of phase (IR2136/IR21363/IR21365) or in phase (IR21362) with inputs.
- Cross-conduction prevention logic
- 3.3V logic compatible
- Lower di/dt gate driver for better noise immunity
- Externally programmable delay for automatic fault clear

Packages



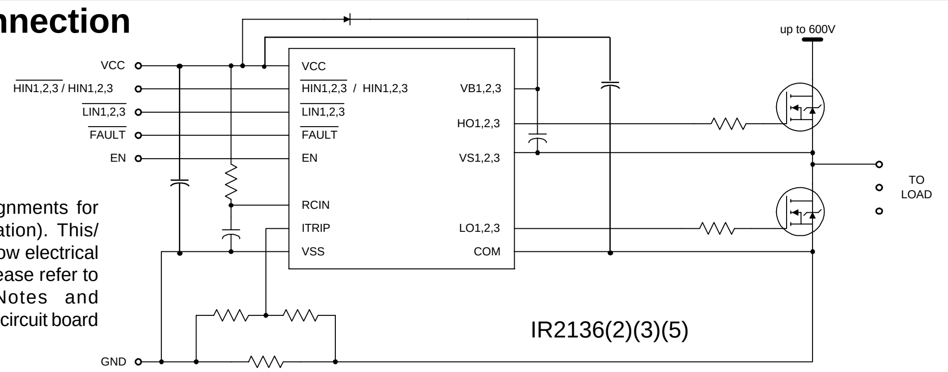
Feature Comparison 2136/21362/21363/21365

Part	Input logic	Under voltage Lockout (VCC, VBS)	Itrip Threshold
2136	$\overline{HIN}$/$\overline{LIN}$	10V	0.46V
21362	HIN/$\overline{LIN}$	11.5V	0.46V
21363	$\overline{HIN}$/$\overline{LIN}$	12V	0.46V
21365	$\overline{HIN}$/$\overline{LIN}$	12V	4.30V

Description

The IR2136/IR21362/IR21363/IR21365(J&S) are high votage, high speed power MOSFET and IGBT drivers with three independent high and low side referenced output channels for 3-phase applications. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 3.3V logic. A current trip function which terminates all six outputs can be derived from an external current sense resistor. An enable function is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that an overcurrent or undervoltage shutdown has occurred. Overcurrent fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600 volts.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/ These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_S	High side offset voltage		$V_{B1,2,3}$ - 25	$V_{B1,2,3}$ + 0.3	V
V_{BS}	High side floating supply voltage		-0.3	625	
V_{HO}	High side floating output voltage		$V_{S1,2,3}$ - 0.3	$V_{B1,2,3}$ + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{SS}	Logic ground		V_{CC} - 25	V_{CC} + 0.3	
$V_{LO1,2,3}$	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Input voltage LIN,HIN,ITRIP, EN, RCIN		V_{SS} - 0.3	lower of (V_{SS} + 15) or V_{CC} + 0.3)	
V_{FLT}	FAULT output voltage		V_{SS} - 0.3	V_{CC} + 0.3	
dV/dt	Allowable offset voltage slew rate		—	50	
P_D	Package power dissipation @ $T_A \leq$ +25°C	(28 lead PDIP)	—	1.5	W
		(28 lead SOIC)	—	1.6	
		(44leadPLCC)	—	2.0	
Rth_{JA}	Thermal resistance, junction to ambient	(28 lead PDIP)	—	83	°C/W
		(28 lead SOIC)	—	78	
		(44 lead PLCC)	—	63	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute referenced to COM. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition		Min.	Max.	Units
$V_{B1,2,3}$	High side floating supply voltage	IR2136	$V_{S1,2,3}$ +10	$V_{S1,2,3}$ +20	V
		IR21362	$V_{S1,2,3}$ +11.5	$V_{S1,2,3}$ +20	
		IR21363/IR21365	$V_{S1,2,3}$ +12	$V_{S1,2,3}$ +20	
$V_{S1,2,3}$	High side floating supply offset voltage		Note 1	600	
$V_{HO1,2,3}$	High side output voltage		$V_{S1,2,3}$	$V_{B1,2,3}$	
$V_{LO1,2,3}$	Low side output voltage		0	V_{CC}	
V_{CC}	Low side and logic fixed supply voltage	IR2136	10	20	
		IR21362	11.5	20	
		IR21363/IR21365	12	20	
V_{SS}	Logic ground		-5	5	
V_{FLT}	FAULT output voltage		V_{SS}	V_{CC}	
V_{RCIN}	RCIN input voltage		V_{SS}	V_{CC}	

Note 1: Logic operational for V_S of COM -5V to COM +600V. Logic state held for V_S of COM -5V to COM $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).
Note 2: All input pins and the ITRIP pin are internally clamped with a 5.2V zener diode.

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute referenced to COM. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_{ITRIP}	ITRIP input voltage	V_{SS}	V_{SS} +5	V
V_{IN}	Logic input voltage $\overline{LIN}$, HIN (IR2136), HIN(IR21362), EN	V_{SS}	V_{SS} +5	
T_A	Ambient temperature	-40	125	°C

Note 2: All input pins and the ITRIP pin are internally clamped with a 5.2V zener diode.

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}1,2,3) = 15V unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels (H_S1,2,3 and L_S1,2,3). The V_O and I_O parameters are referenced to COM and V_S1,2,3 and are applicable to the respective output leads: $H_{O1,2,3}$ and $L_{O1,2,3}$.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "0" input voltage $\overline{LIN1,2,3}$, $\overline{HIN1,2,3}$ Logic "1" input voltage HIN1,2,3	3	—	—		
V_{IL}	Logic "1" input voltage $\overline{LIN1,2,3}$, $\overline{HIN1,2,3}$ Logic "0" input voltage HIN1,2,3	—	—	0.8		
$V_{EN,TH+}$	EN positive going threshold	—	—	3		
$V_{EN,TH-}$	EN negative going threshold	0.8	—	—		
$V_{IT,TH+}$	ITRIP positive going threshold IR21361/IR21362/IR21363	0.37	0.46	0.55		
	IR21365	3.85	4.30	4.75		
$V_{IT,HYS}$	ITRIP input hysteresis IR21361/IR21362/IR21363	—	0.07	—		
	IR21365	—	.15	—		
$V_{RCIN,TH+}$	RCIN positive going threshold	—	8	—	V	
$V_{RCIN,HYS}$	RCIN input hysteresis	—	3	—		
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	0.9	1.4		I_O = 20 mA
V_{OL}	Low level output voltage, V_O	—	0.4	0.6		I_O = 20 mA
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold IR2136	8.0	8.9	9.8		
	IR21362	9.6	10.4	11.2		
	IR21363/IR21365	10.6	11.1	11.6		
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold IR2136	7.4	8.2	9.0		
	IR21362	8.6	9.4	10.2		
	IR21363/IR21365	10.4	10.9	11.4		
V_{CCUVH} V_{BSUVH}	V_{CC} and V_{BS} supply undervoltage lockout hysteresis IR2136	0.3	0.7	—		
	IR21362	0.5	1.0	—		
	IR21363/IR21365	—	0.2	—	µA	
I_{LK}	Offset supply leakage current	—	—	50		$V_{B1,2,3}$=$V_{S1,2,3}$=600V
I_{QBS}	Quiescent V_{BS} supply current	—	70	120		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	—	1.6	2.3	mA	
$V_{IN, CLAMP}$	Input clamp voltage (HIN, LIN, ITRIP and EN)	4.9	5.2	5.5	V	I_{IN} =100µA
I_{LIN+}	Input bias current (LOUT = HI)	—	200	300	µA	V_{LIN} = 0V

Static Electrical Characteristics cont.

V_{BIAS} (V_{CC}, V_{BS}1,2,3) = 15V unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels (H_S1,2,3 and L_S1,2,3). The V_O and I_O parameters are referenced to COM and V_S1,2,3 and are applicable to the respective output leads: $H_{O1,2,3}$ and $L_{O1,2,3}$.

Symbol	Definition		Min.	Typ.	Max.	Units	Test Conditions
I_{LIN-}	Input bias current (LOUT = LO)		—	100	220	µA	V_{LIN} = 5V
I_{HIN+}	Input bias current (HOUT = HI)	IR2136(3)(5)	—	200	300		V_{HIN} = 0V
		IR21362	—	30	100		V_{HIN} = 5V
I_{HIN-}	Input bias current (HOUT = LO)	IR2136(3)(5)	—	100	220		V_{HIN} = 5V
		IR21362	—	0	1		V_{HIN} = 0V
I_{ITRIP+}	"high" ITRIP input bias current		—	30	100		V_{ITRIP} = 5V
I_{ITRIP-}	"low" ITRIP input bias current		—	0	1		V_{ITRIP} = 0V
I_{EN+}	"high" ENABLE input bias current		—	30	100		V_{ENABLE}= 5V
I_{EN-}	"low" ENABLE input bias current		—	0	1		V_{ENABLE} = 0V
I_{RCIN}	RCIN input bias current		—	0	1		V_{RCIN} = 0V or 15V
I_{O+}	Output high short circuit pulsed current		120	200	—	mA	V_O=0V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current		250	350	—		V_O=15V, PW ≤10 µs
$R_{ON,RCIN}$	RCIN low on resistance		—	50	100	Ω	
$R_{ON,FLT}$	FAULT low on resistance		—	50	100		

Dynamic Electrical Characteristics

V_{CC} = V_{BS} = V_{BIAS} = 15V, $V_{S1,2,3}$ = V_{SS} = COM, TA = 25ºC and C_L = 1000 pF unless otherwise specified.

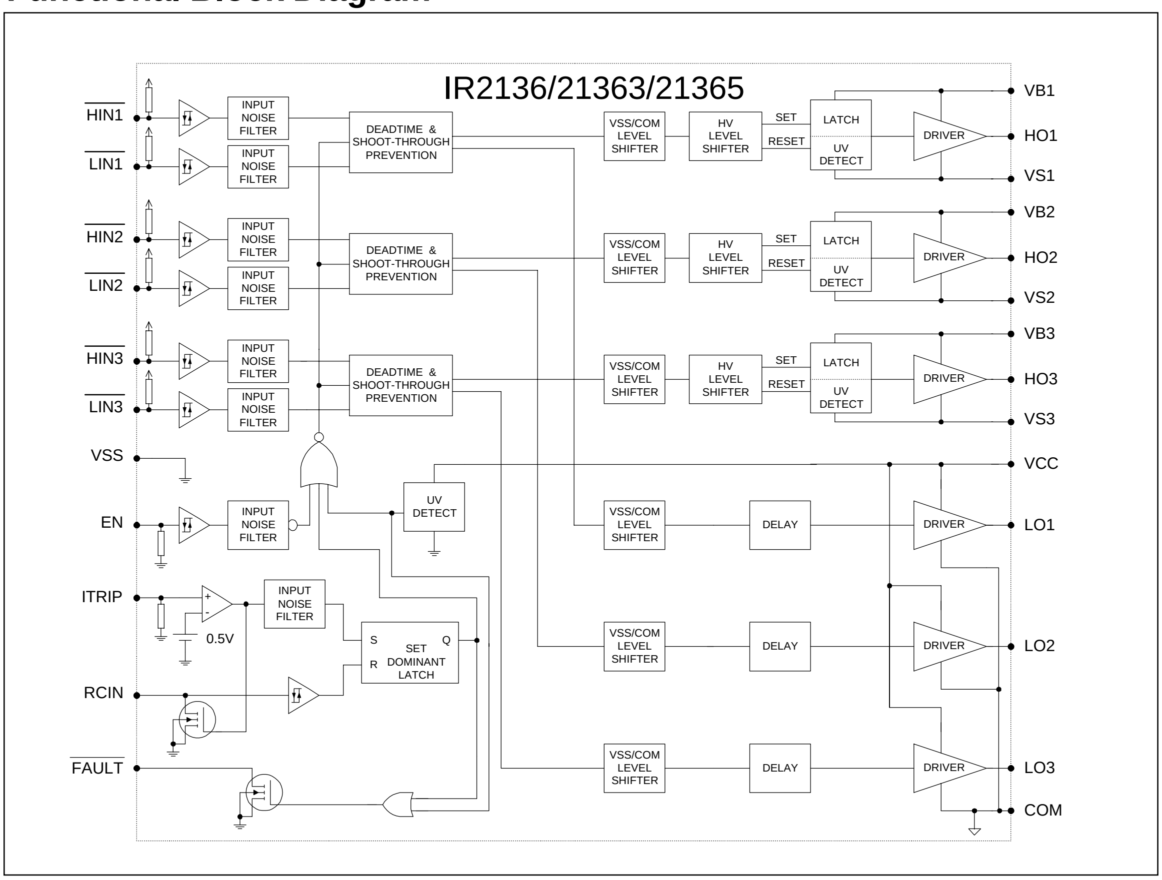
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	300	425	550	nS	V_{IN} = 0 & 5V $V_{S1,2,3}$ = 0 to 600V
t_{off}	Turn-off propagation delay	250	400	550		
t_r	Turn-on rise time	—	125	190		
t_f	Turn-off fall time	—	50	75		
t_{EN}	ENABLE low to output shutdown propagation delay	300	450	600		V_{IN}, V_{EN} = 0V or 5V
t_{ITRIP}	ITRIP to output shutdown propagation delay	500	750	1000		V_{ITRIP} = 5V
t_{bl}	ITRIP blanking time	100	150	—		V_{IN} = 0V or 5V V_{ITRIP} = 5V
t_{FLT}	ITRIP to FAULT propagation delay	400	600	800		V_{IN} = 0V or 5V V_{ITRIP} = 5V
t_{FILIN}	Input filter time (HIN, LIN, EN)	100	200	—		V_{IN} = 0 & 5V
t_{FLTCLR}	FAULT clear time RCIN: R=2meg, C=1nF	1.3	1.65	2	mS	V_{IN} = 0V or 5V V_{ITRIP} = 0V
DT	Deadtime	220	290	360	nS	V_{IN} = 0 & 5V
MT	Matching delay ON and OFF	—	40	75		
MDT	Matching delay, max (t_{on},t_{off}) - min (t_{on},t_{off}), (ton,toff are applicable to all 3 channels)	—	25	70		External dead time >400nsec
PM	Output pulse width matching, PWin - PWout (fig.2)	—	40	75		

NOTE: For high side PWM, HIN pulse width must be ≥ 1µsec

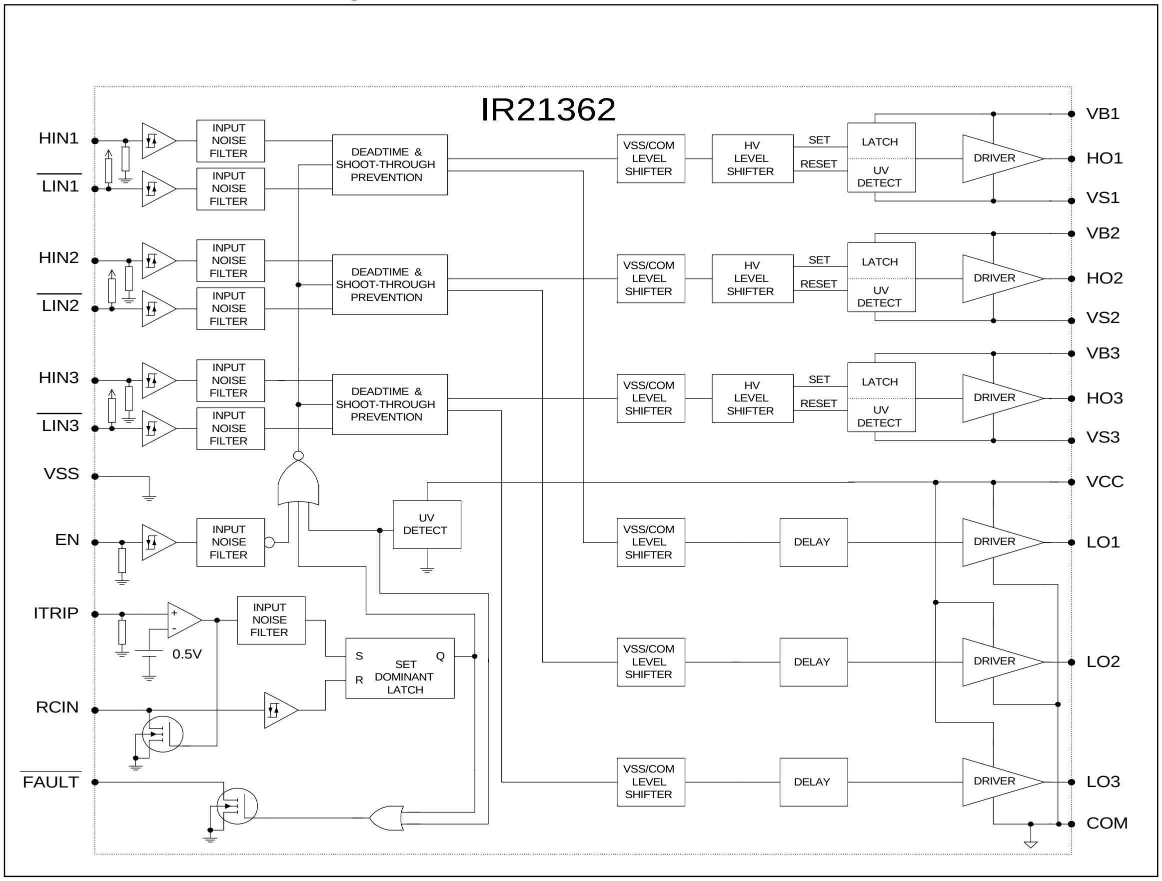
VCC	VBS	ITRIP	ENABLE	FAULT	LO1,2,3	HO1,2,3
<UVCC	X	X	X	0 (note 1)	0	0
15V	<UVBS	0V	5V	high imp	LIN1,2,3	0
15V	15V	0V	5V	high imp	LIN1,2,3	HIN1,2,3
15V	15V	>V_{ITRIP}	5V	0 (note 2)	0	0
15V	15V	0V	0V	high imp	0	0

Note: A shoot-through prevention logic prevents LO1,2,3 and HO1,2,3 for each channel from turning on simultaneously.
Note 1: UVCC is not latched, when VCC>UVCC, FAULT returns to high impedance.
Note 2: When ITRIP <V_{ITRIP}, FAULT returns to high-impedance after RCIN pin becomes greater than 8V (@ VCC = 15V)

Functional Block Diagram



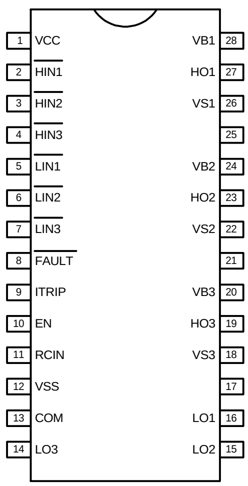
Functional Block Diagram



Lead Definitions

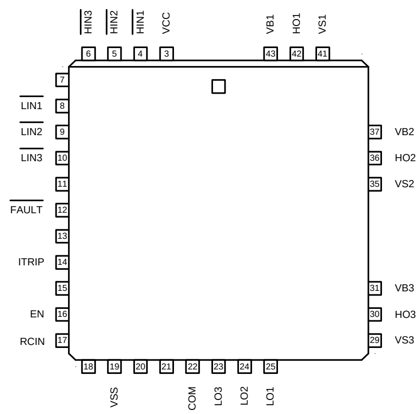
Symbol	Description
V_{CC}	Low side and logic fixed supply
VSS	Logic Ground
$\overline{HIN1,2,3}$ HIN1,2,3	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase (IR2136/IR21363IR21365) Logic inputs for high side gate driver outputs (HO1,2,3), in phase (IR21362)
$\overline{LIN1,2,3}$	Logic inputs for low side gate driver outputs (LO1,2,3), out of phase
FAULT	Indicates over-current (ITRIP) or low-side undervoltage lockout has occured. Negative logic, open-drain output
EN	Logic input to enable I/O functionality. Positive logic, i.e. I/O logic functions when ENABLE is high. No effect on FAULT and not latched
ITRIP	Analog input for overcurrent shutdown. When active, ITRIP shuts down outputs and activates FAULT and RCIN low. When ITRIP becomes inactive, FAULT stays active low for an externally set time T_{FLTCLR}, then automatically becomes inactive (open-drain high impedance).
RCIN	External RC network input used to define FAULT CLEAR delay, T_{FLTCLR}, approximately equal to R*C. When RCIN>8V, the FAULT pin goes back into open-drain high-impedance
COM	Low side gate driver return
V_B1,2,3	High side floating supply
HO1,2,3	High side gate driver outputs
$V_{S1,2,3}$	High voltage floating supply returns
LO1,2,3	Low side gate driver output

Lead Assignments



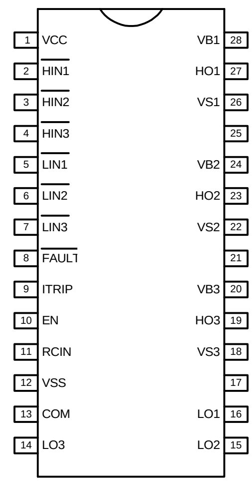
28 Lead PDIP

IR2136/IR21363/IR21365



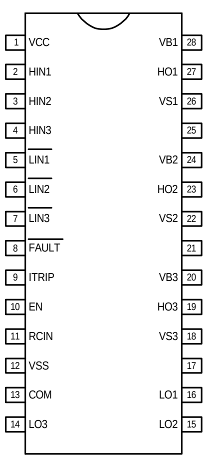
44 Lead PLCC w/o 12 leads

IR2136/IR21363/IR21365 (J)



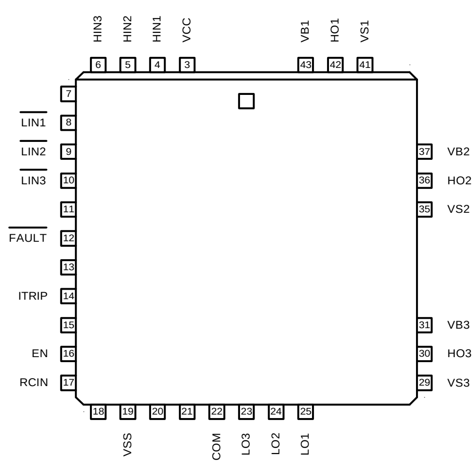
28 lead SOIC (wide body)

IR2136/IR21363/IR21365 (S)



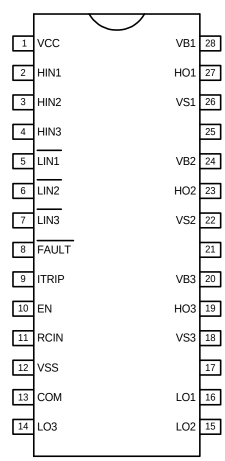
28 Lead PDIP

IR21362



44 Lead PLCC w/o 12 leads

IR21362J



28 lead SOIC (wide body)

IR21362S

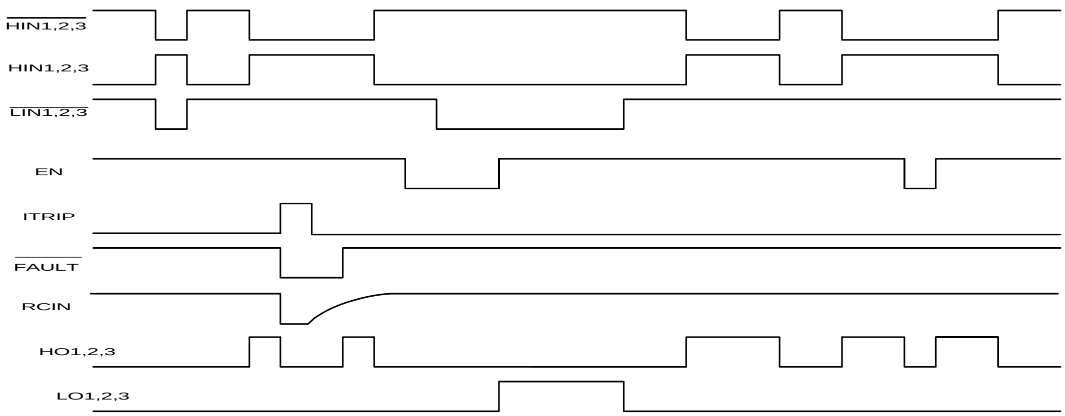


Figure 1. Input/Output Timing Diagram

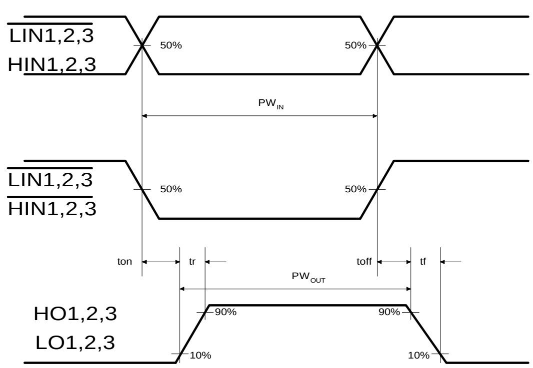


Figure 2. Switching Time Waveforms

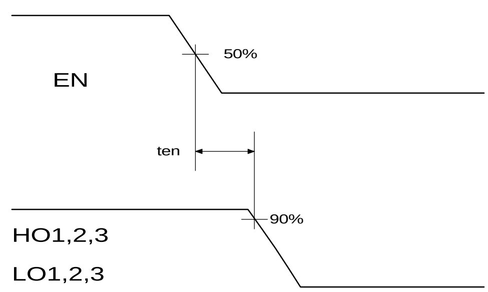


Figure 3. Output Enable Timing Waveform

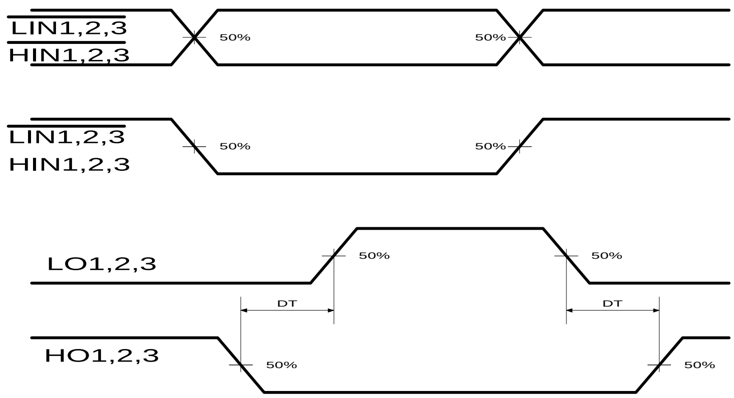


Figure 4. Internal Deadtime Timing Waveforms

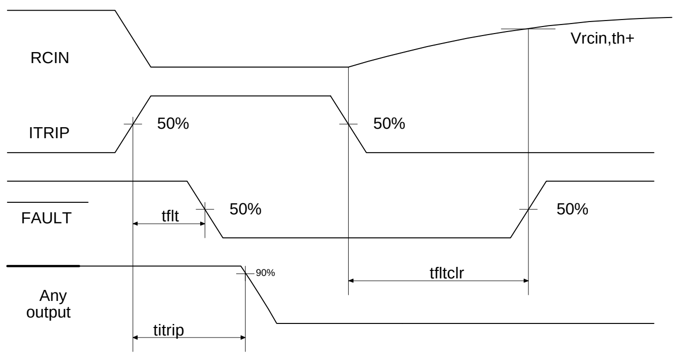


Figure 5. ITRIP/RCIN Timing Waveforms

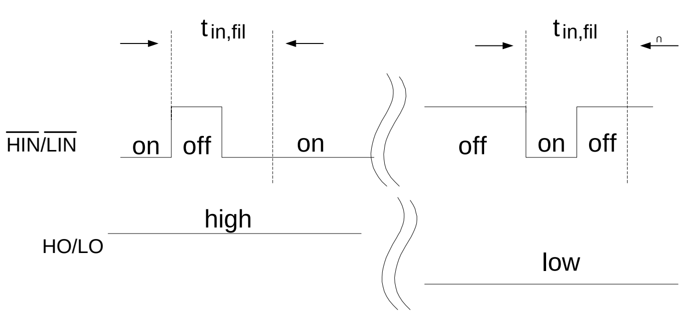


Figure 5.5 Input Filter Function

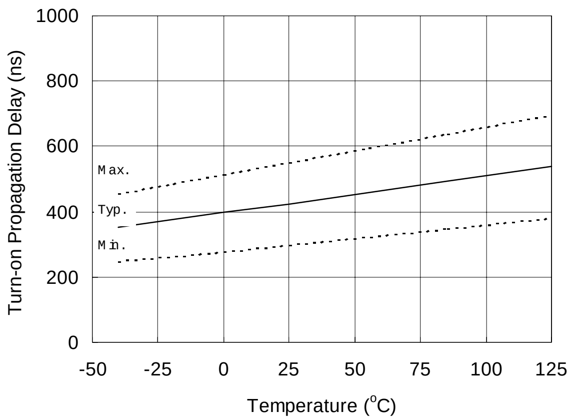


Figure 6A. Turn-on Propagation Delay vs. Temperature

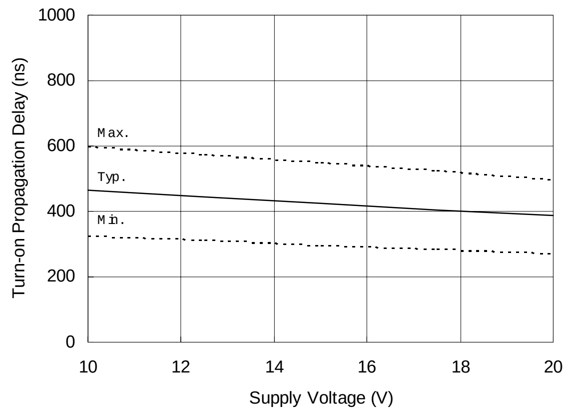


Figure 6B. Turn-on Propagation Delay vs. Supply Voltage

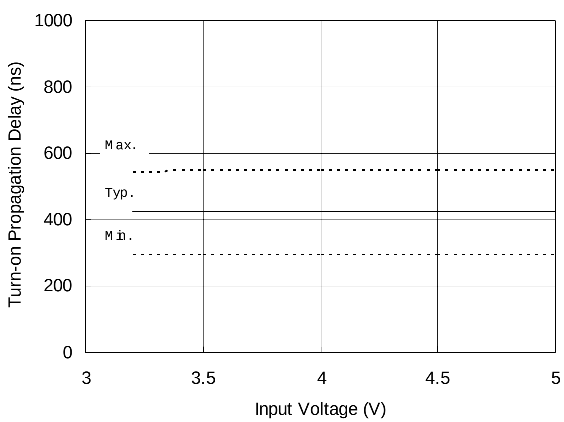


Figure 6C. Turn-on Propagation Delay vs. Input Voltage

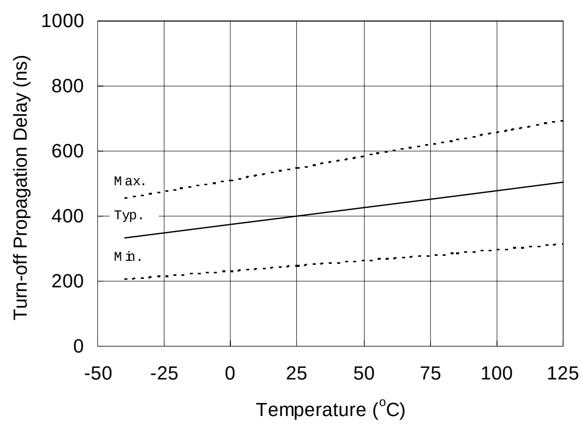


Figure 7A. Turn-off Propagation Delay vs. Temperature

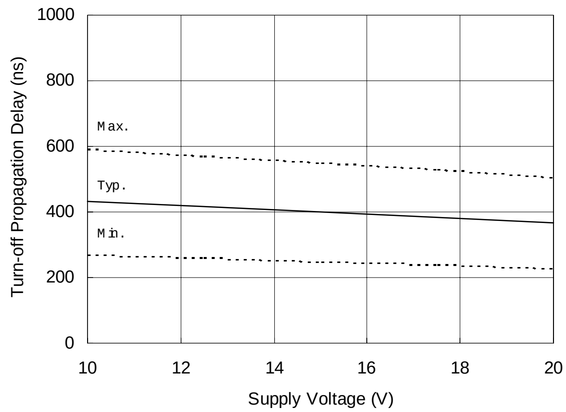


Figure 7B. Turn-off Propagation Delay vs. Supply Voltage

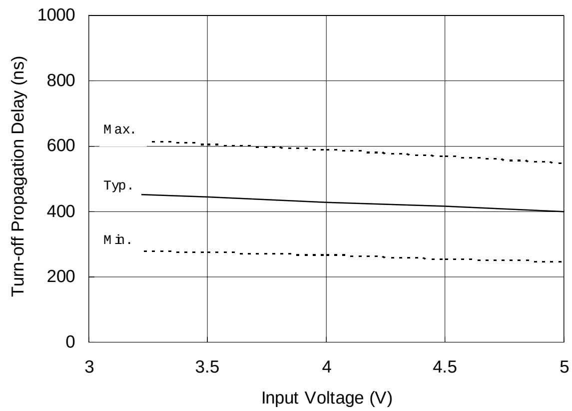


Figure 7C. Turn-off Propagation Delay vs. Input Voltage

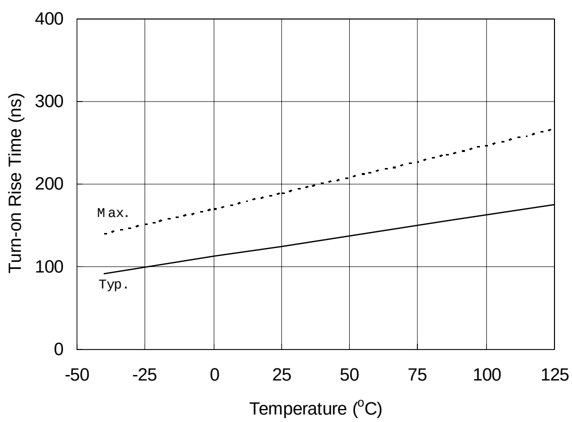


Figure 8A. Turn-on Rise Time vs. Temperature

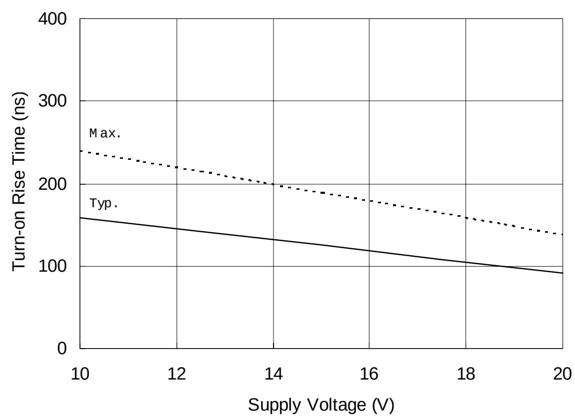


Figure 8B. Turn-on Rise Time vs. Supply Voltage

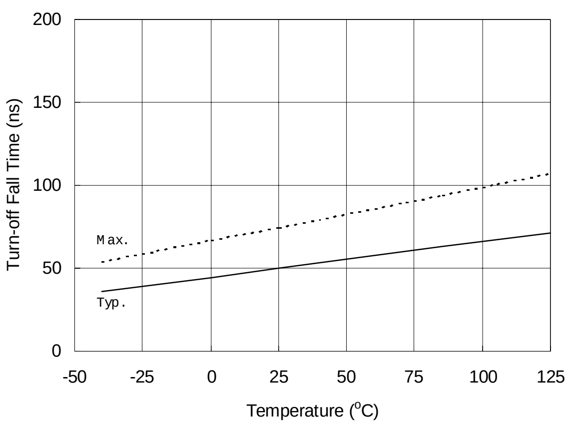


Figure 9A. Turn-off Fall Time vs. Temperature

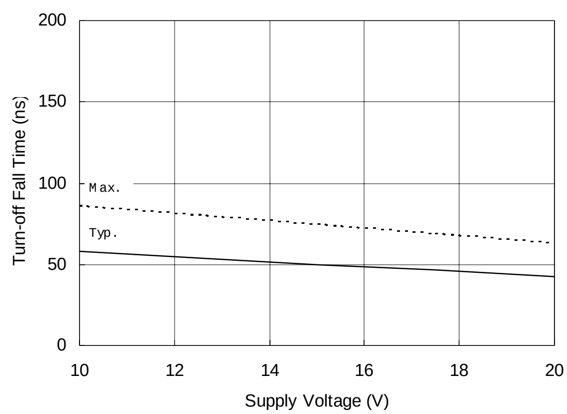


Figure 9B. Turn-off Fall Time vs. Supply Voltage

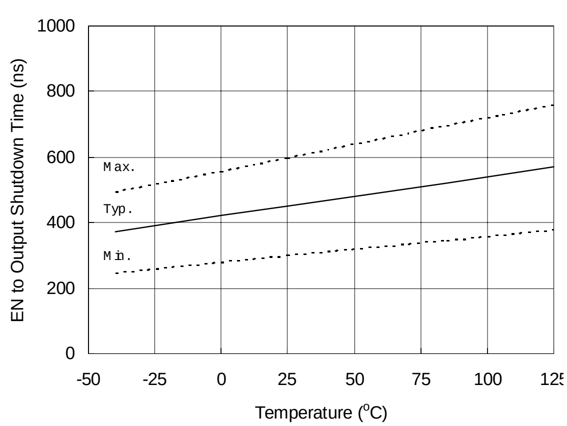


Figure 10A. EN to Output Shutdown Time vs. Temperature

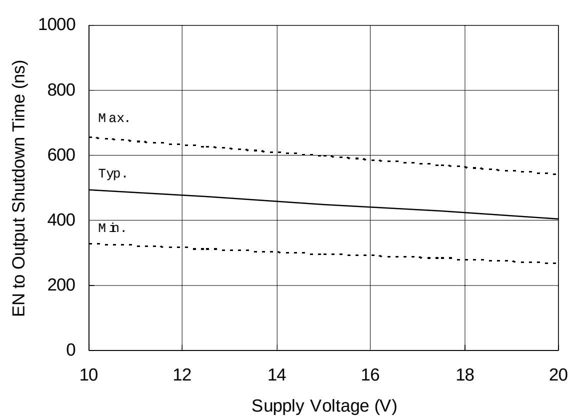


Figure 10B. EN to Output Shutdown Time vs. Supply Voltage

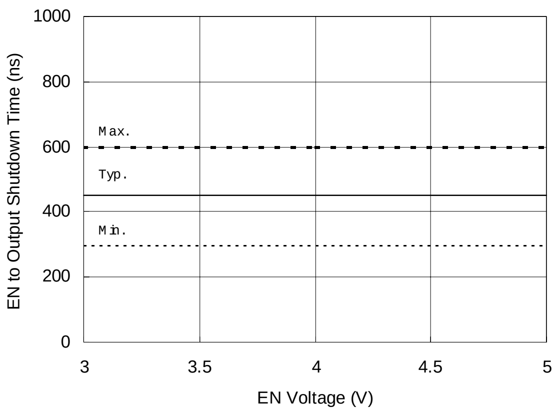


Figure 10C. EN to Output Shutdown Time vs. EN Voltage

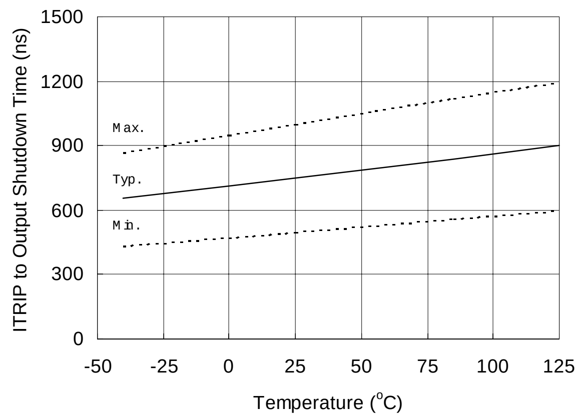


Figure 11A. ITRIP to Output Shutdown Time vs. Temperature

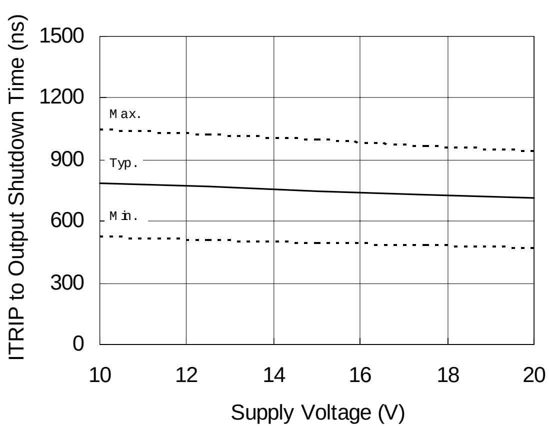


Figure 11B. ITRIP to Output Shutdown Time vs. Supply Voltage

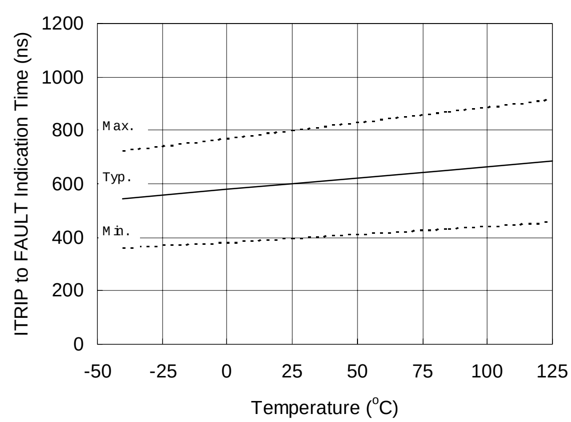


Figure 12A. ITRIP to FAULT Indication Time vs. Temperature

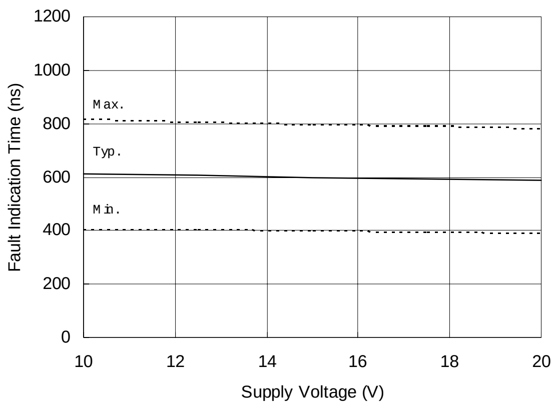


Figure 12B. ITRIP to FAULT Indication Time vs. Supply Voltage

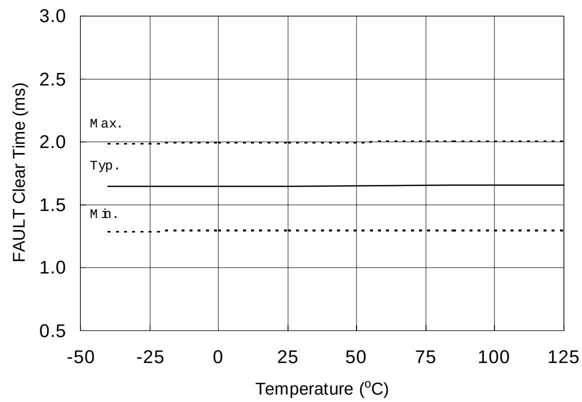


Fig13A. FAULT Clear Time vs. Temperature

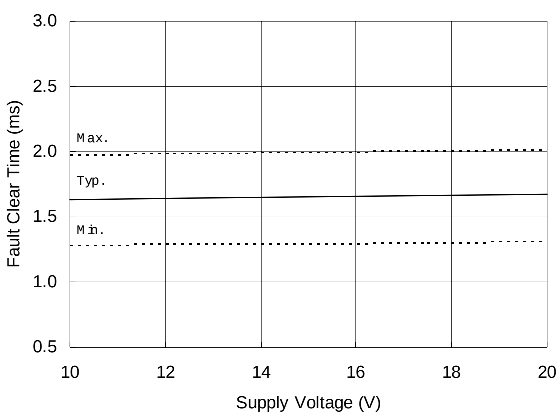


Figure 13B. FAULT Clear Time vs. Supply Voltage

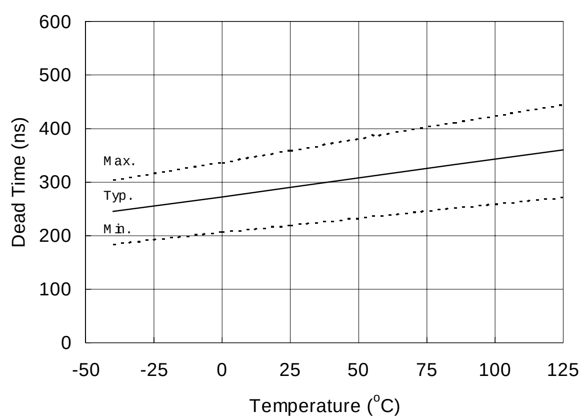


Figure 14A. Dead Time vs. Temperature

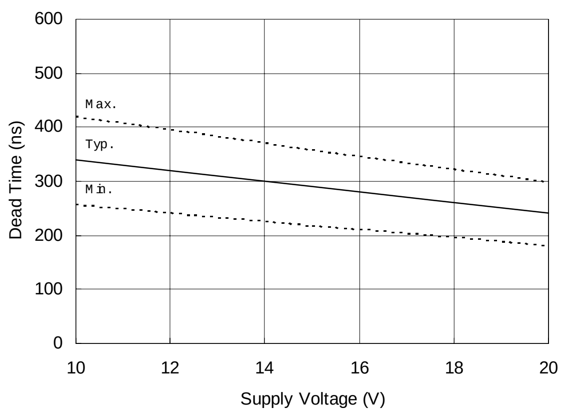


Figure 14B. Dead Time Time vs. Supply Voltage

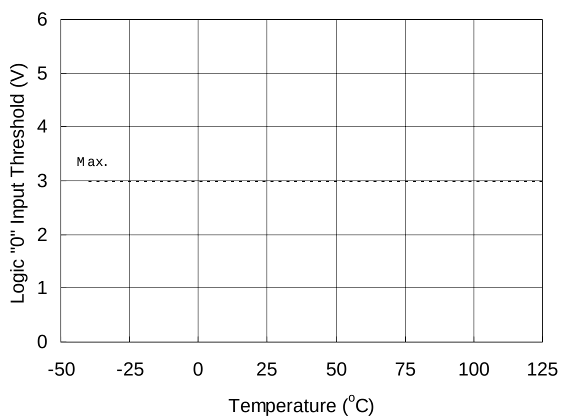


Figure 15A. Logic "0" Input Threshold vs. Temperature

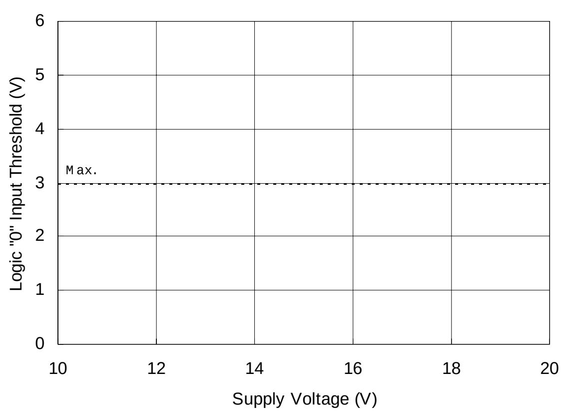


Figure 15B. Logic "0" Input Threshold vs. Supply Voltage

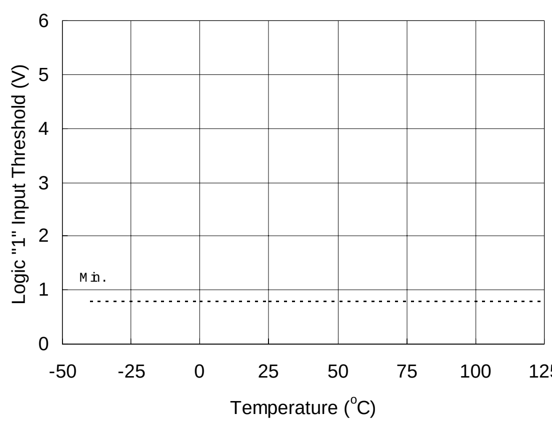


Figure 16A. Logic "1" Input Threshold vs. Temperature

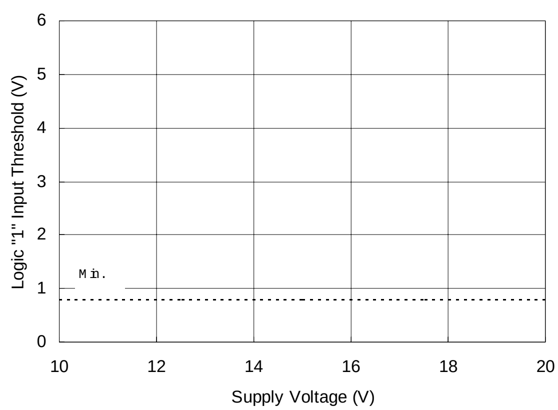


Figure 16B. Logic "1" Input Threshold vs. Supply Voltage

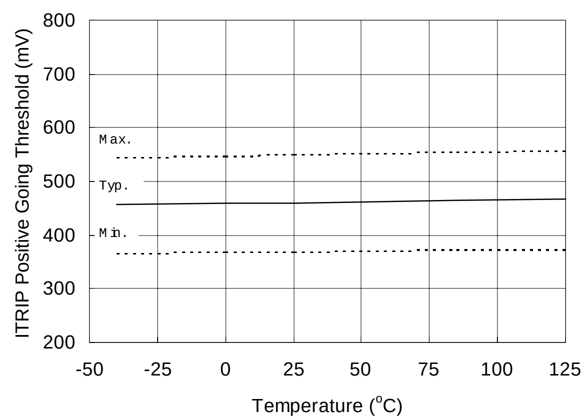


Figure 17A. ITRIP Positive Going Threshold vs. Temperature (IR2136/21362/21363 Only)

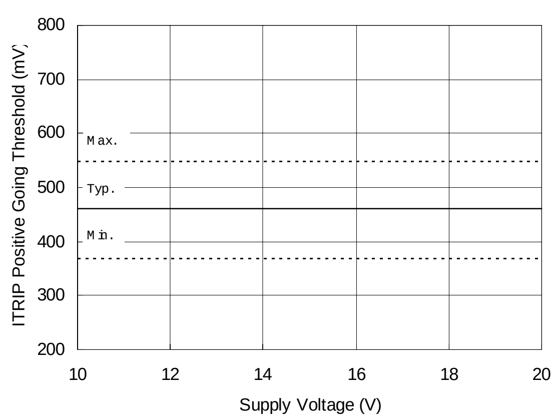


Figure 17B. ITRIP Positive Going Threshold vs. Supply Voltage (IR2136/21362/21363 Only)

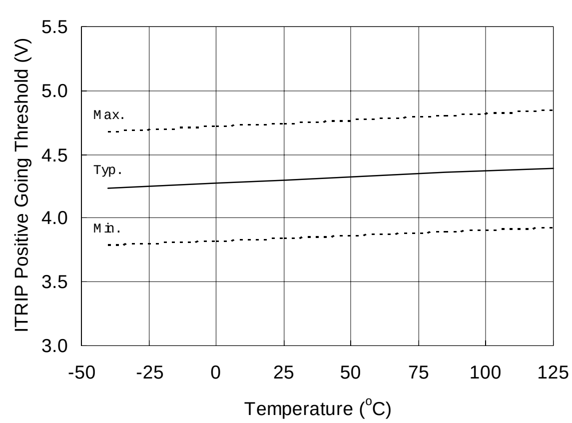


Figure 17C. ITRIP Positive Going Threshold vs. Temperature (IR21365 Only)

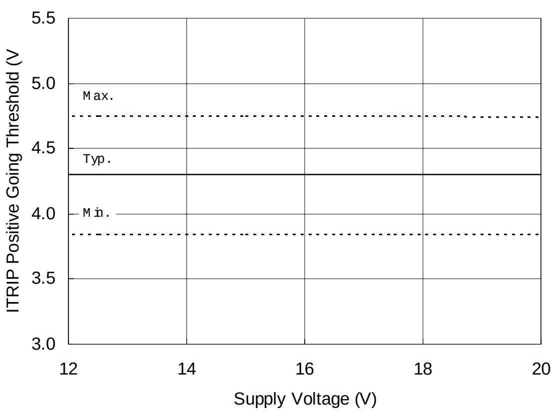


Figure 17D. ITRIP Positive Going Threshold vs. Supply Voltage (IR21365 Only)

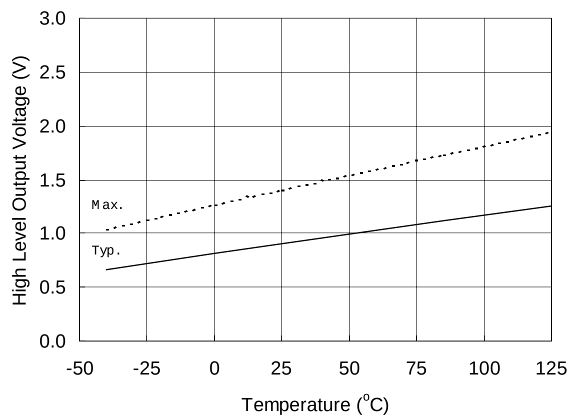


Figure 18A. High Level Output vs. Temperature

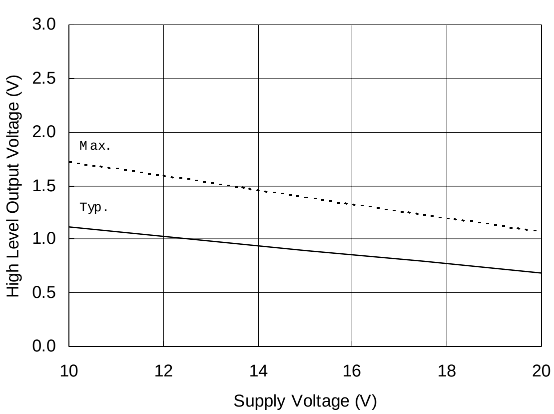


Figure 18B. High Level Output vs. Supply Voltage

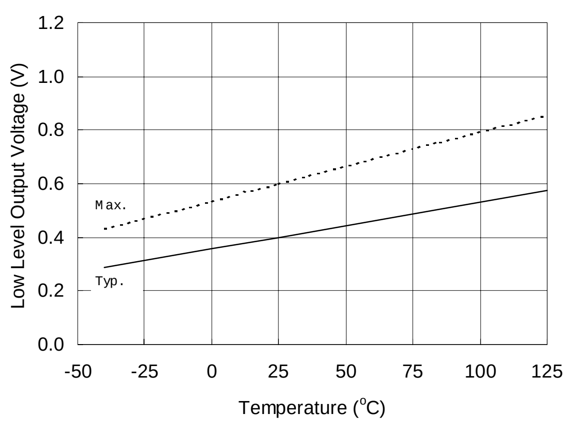


Figure 19A. Low Level Output vs. Temperature

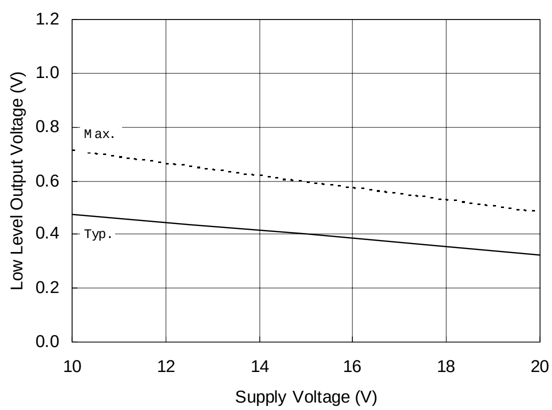


Figure 19B. Low Level Output vs. Supply Voltage

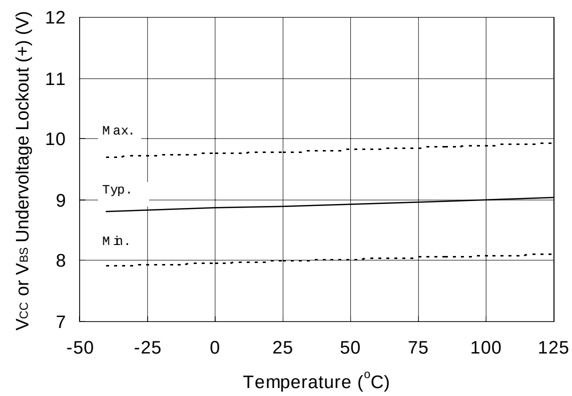


Figure 20. V_{CC} or V_{BS} Undervoltage (+) vs. Temperature (IR2136 Only)

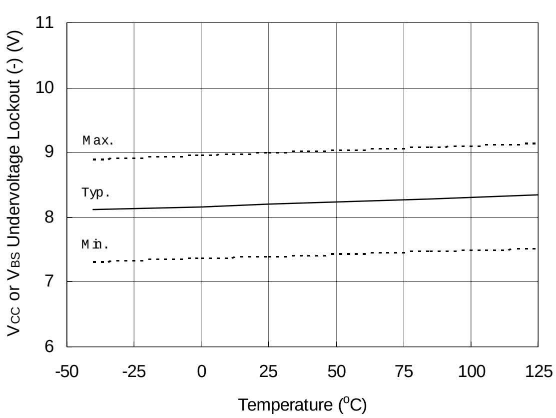


Figure 21. V_{CC} or V_{BS} Undervoltage (-) vs. Temperature (IR2136 Only)

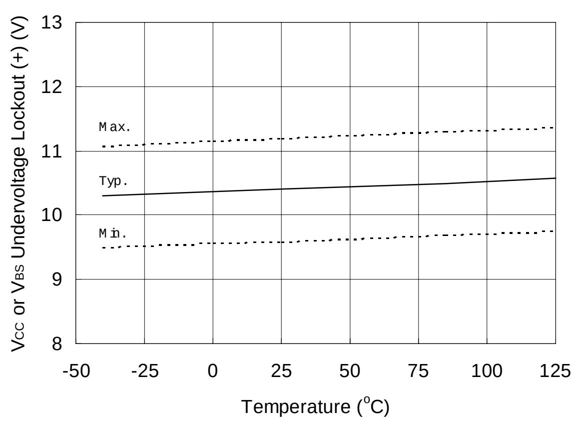


Figure 22. V_{CC} or V_{BS} Undervoltage (+) vs. Temperature (IR21362 Only)

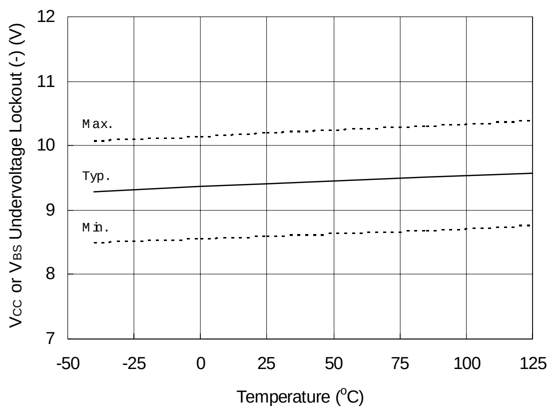


Figure 23. V_{CC} or V_{BS} Undervoltage (-) vs. Temperature (IR21362 Only)

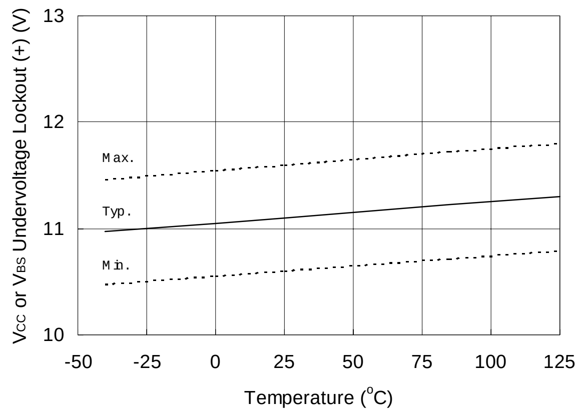


Figure 24. V_{CC} or V_{BS} Undervoltage (+) vs. Temperature (IR21363/21365 Only)

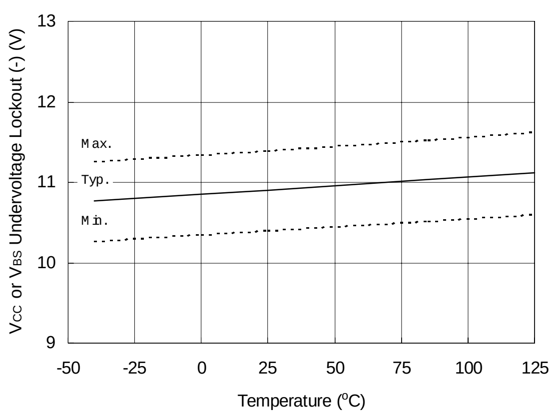


Figure 25. V_{CC} or V_{BS} Undervoltage (-) vs. Temperature (IR21363/21365 Only)

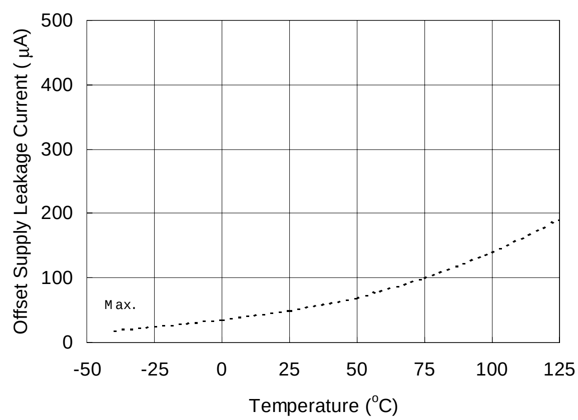


Figure 26A. Offset Supply Leakage Current vs. Temperature

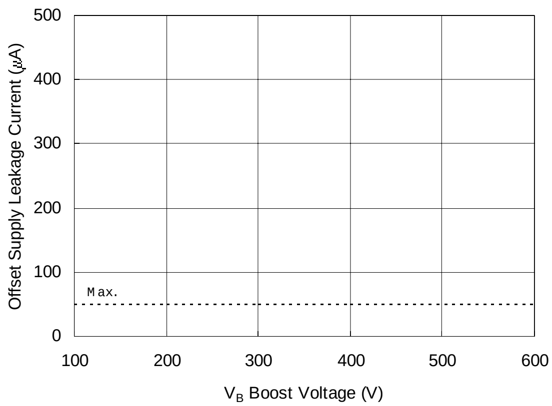


Figure 26B. Offset Supply Leakage Current vs. V_B Boost Voltage

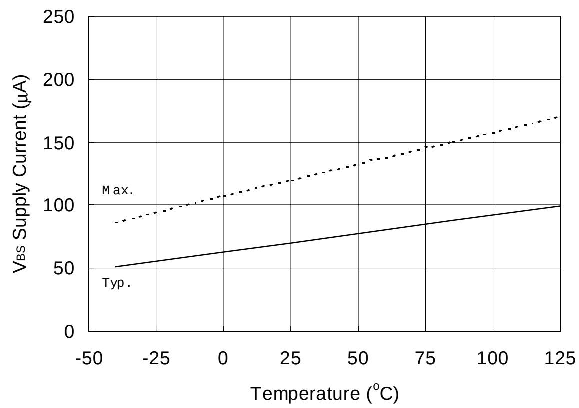


Figure 27A. V_{BS} Supply Current vs. Temperature

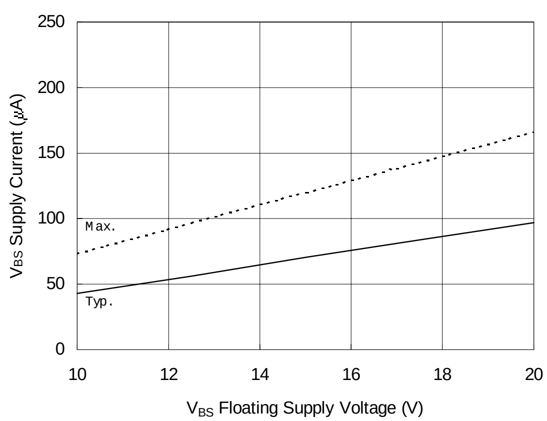


Figure 27B. V_{BS} Supply Current vs. V_{BS} Floating Supply Voltage

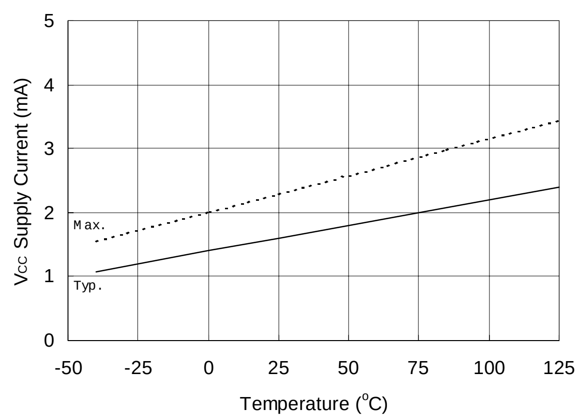


Figure 28A. V_{CC} Supply Current vs. Temperature

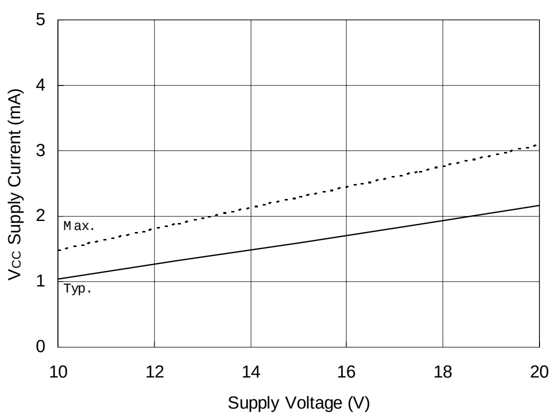


Figure 28B. V_{CC} Supply Current vs. V_{CC} Supply Voltage

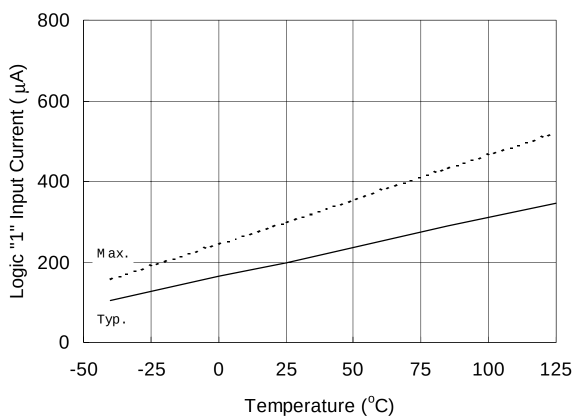


Figure 29A. Logic "1" Input Current vs. Temperature (IR2136/21363/21365 and IR21362 Low Side Only)

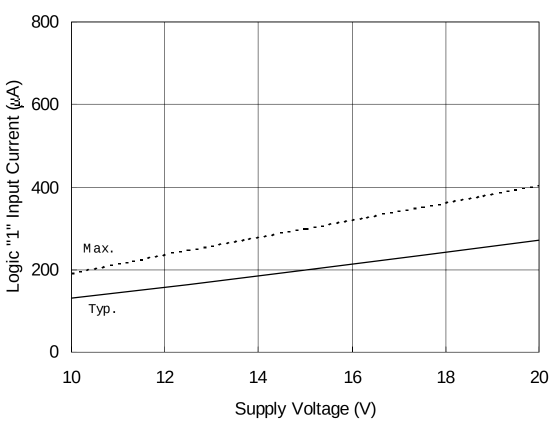


Figure 29B. Logic "1" Input Current vs. Supply Voltage (IR2136/21363/21365 and IR21362 Low Side Only)

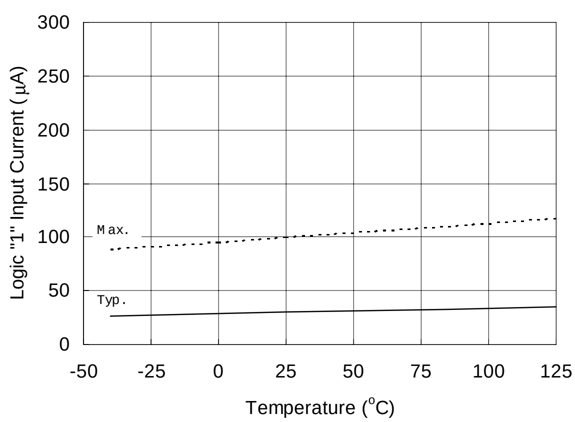


Figure 29C. Logic "1" Input Current vs. Temperature (IR21362 High Side Only)

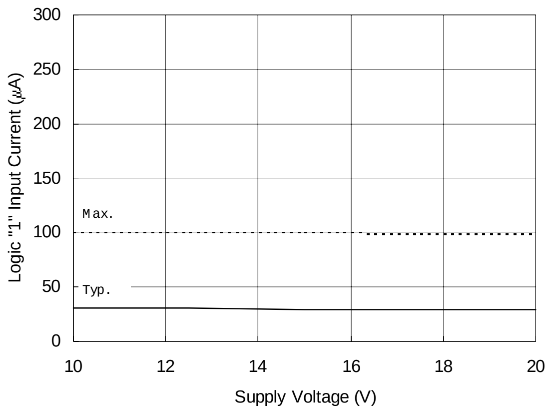


Figure 29D. Logic "1" Input Current vs. Supply Voltage (IR21362 High Side Only)

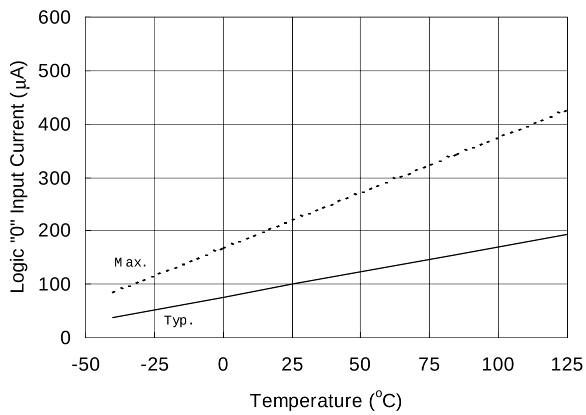


Figure 30A. Logic "0" Input Current vs. Temperature (IR2136/21363/21365 and IR21362 Low Side Only)

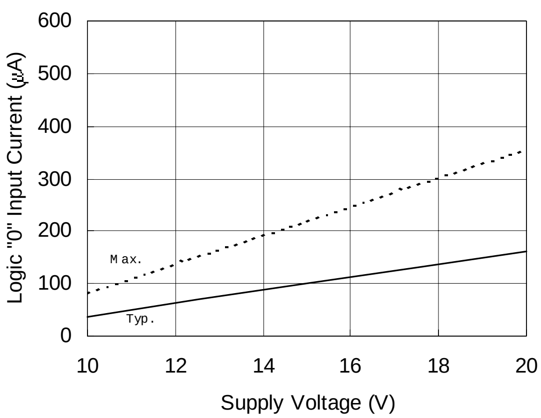


Figure 30B. Logic "0" Input Current vs. Supply Voltage (IR2136/21363/21365 and IR21362 Low Side Only)

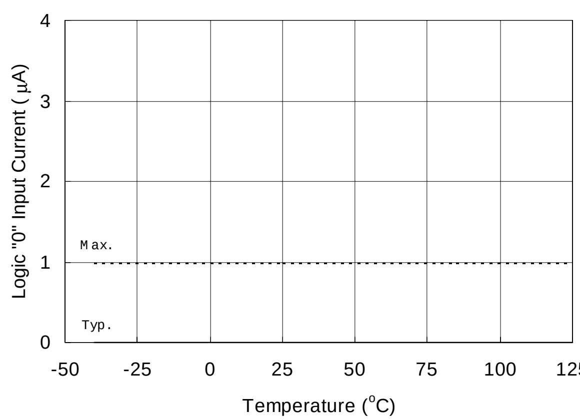


Figure 30C. Logic "0" Input Current vs. Temperature (IR21362 High Side Only)

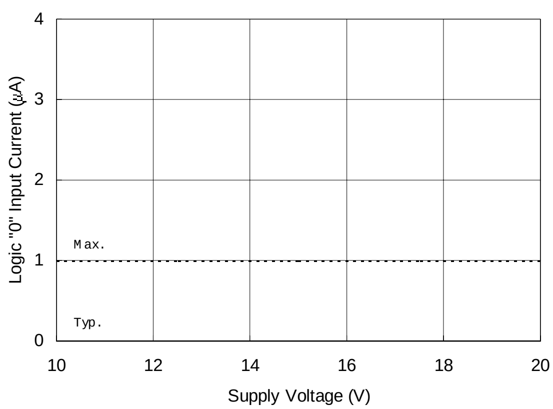


Figure 30D. Logic "0" Input Current vs. Supply Voltage (IR21362 High Side Only)

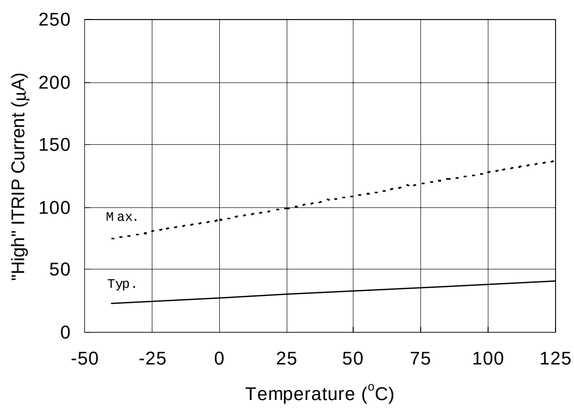


Figure 31A. "High" ITRIP Current vs. Temperature

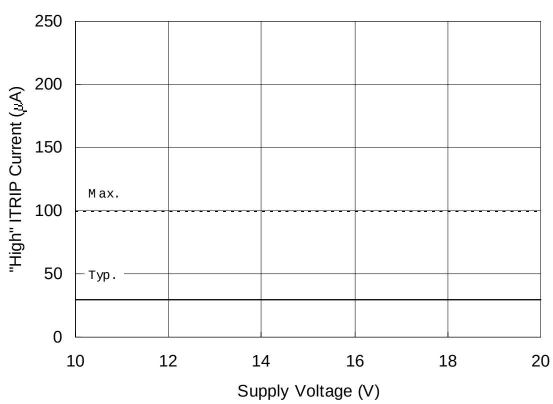


Figure 31B. "High" ITRIP Current vs. Supply Voltage

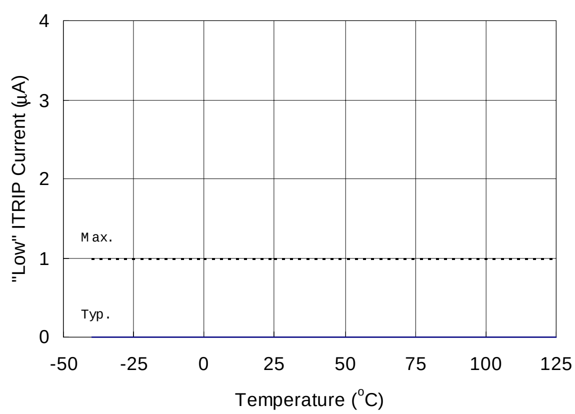


Figure 32A. "Low" ITRIP Current vs. Temperature

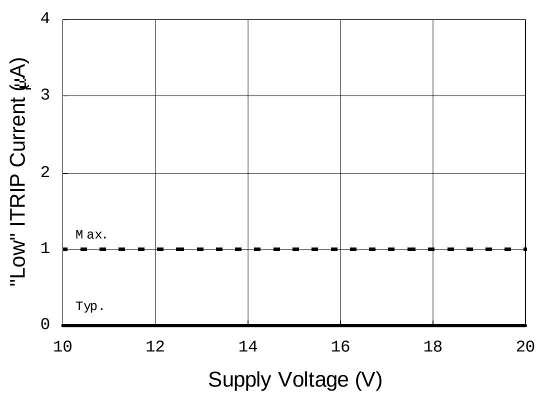


Figure 32B. "Low" ITRIP Current vs. Supply Voltage

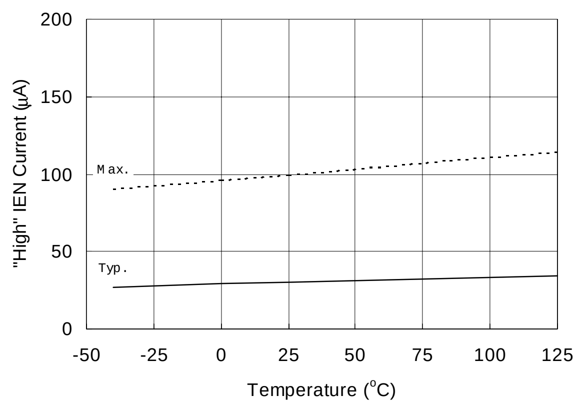


Figure 33A. "High" IEN Current vs. Temperature

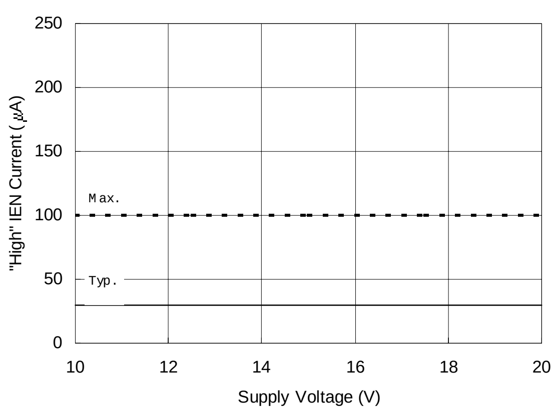


Figure 33B. "High" IEN Current vs. Supply Voltage

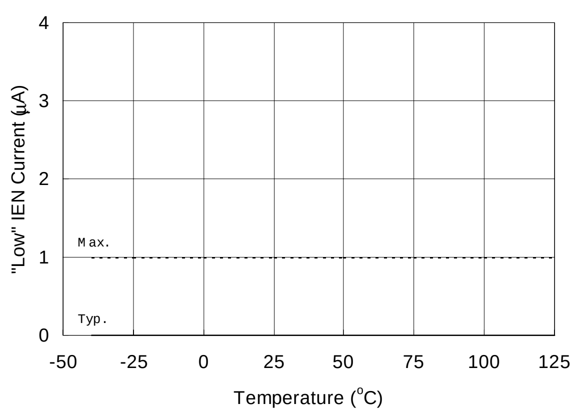


Figure 34A. "Low" IEN Current vs. Temperature

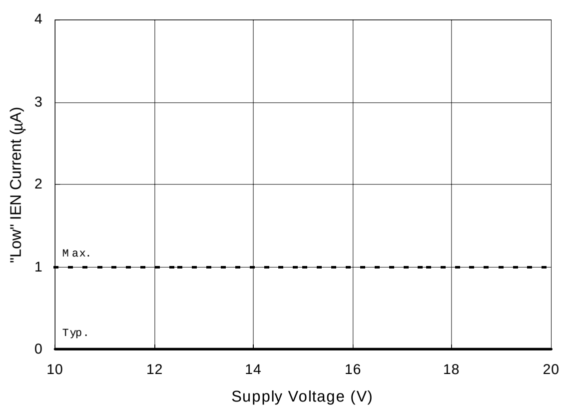


Figure 34B. "Low" IEN Current vs. Supply Voltage

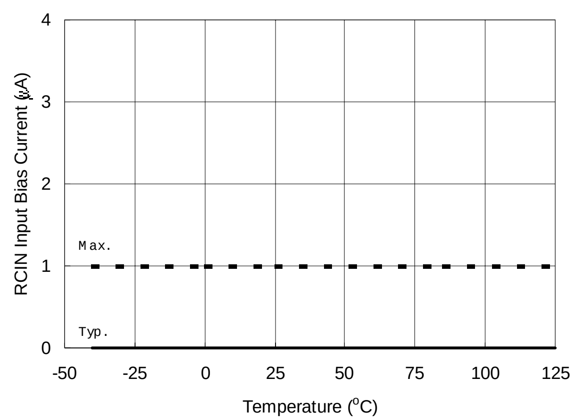


Figure 35A. RCIN Input Bias Current vs. Temperature

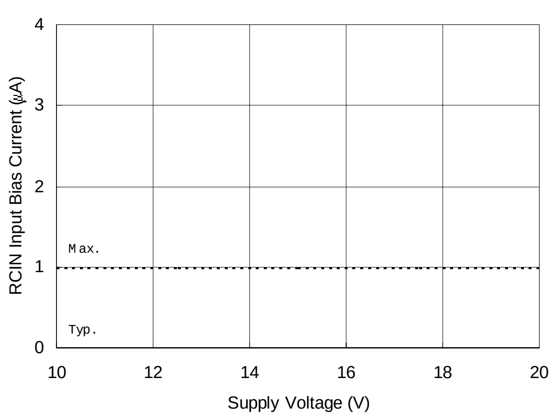


Figure 35B. RCIN Input Bias Current vs. Supply Voltage

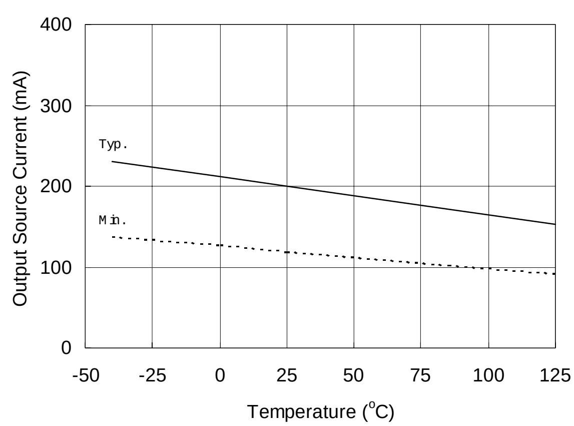


Figure 36A. Output Source Current vs. Temperature

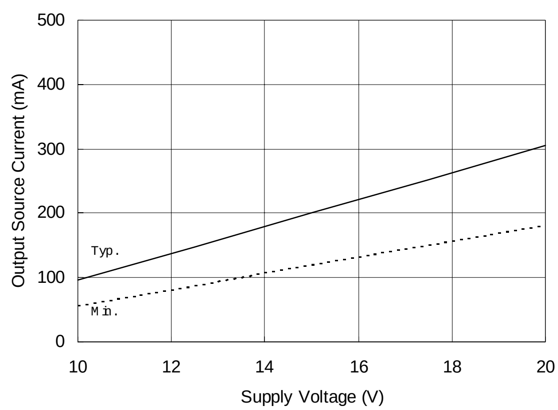


Figure 36B. Output Source Current vs. Supply Voltage

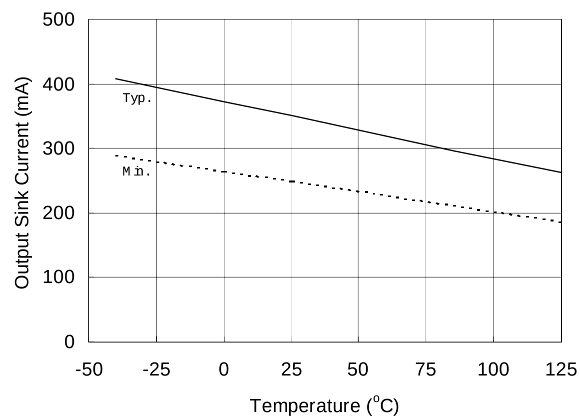


Figure 37A. Output Sink Current vs. Temperature

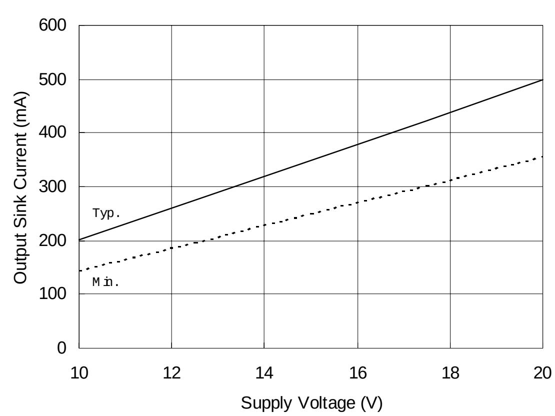


Figure 37B. Output Sink Current vs. Supply Voltage

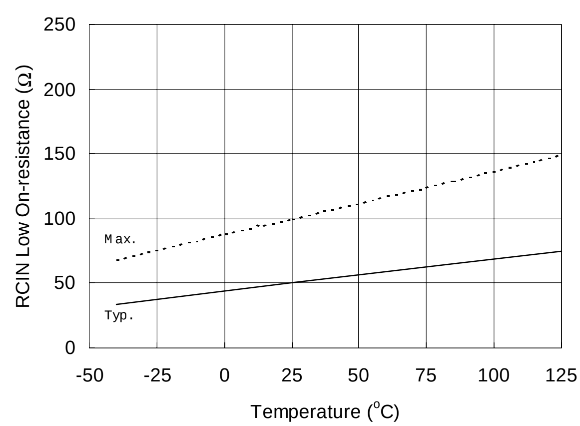


Figure 38A. RCIN Low On-resistance vs. Temperature

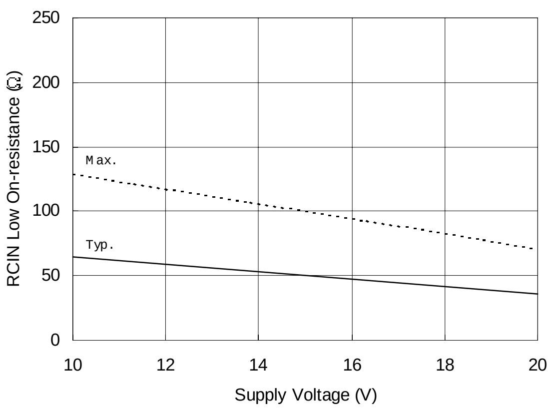


Figure 38B. RCIN Low On-resistance vs. Supply Voltage

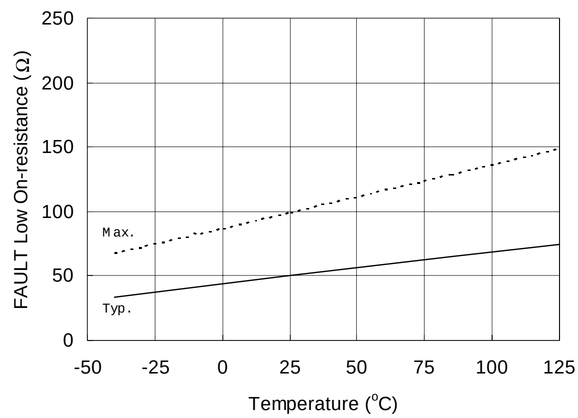


Figure 39A. FAULT Low On-resistance vs. Temperature

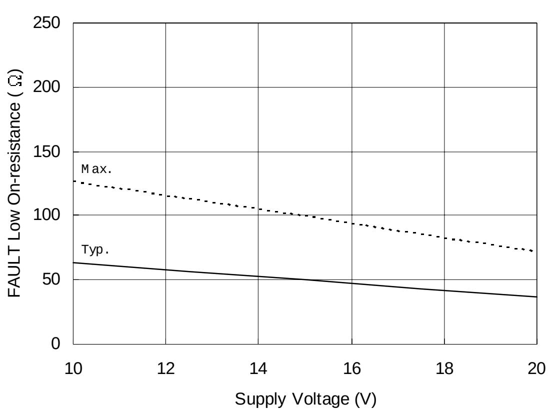


Figure 39B. FAULT Low On-resistance vs. Supply Voltage

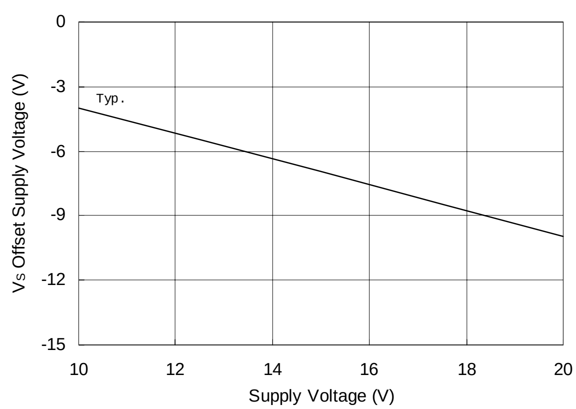


Figure 40. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage

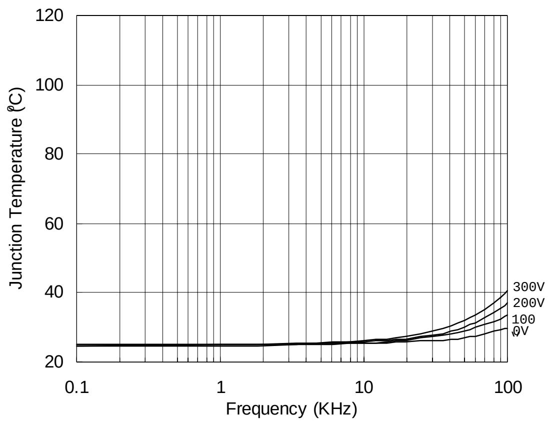


Figure 41. IR2136/IR21362/IR21363/IR21365 vs. Frequency (IRG4BC20W), R_{gate}=33Ω, V_{CC}=15V

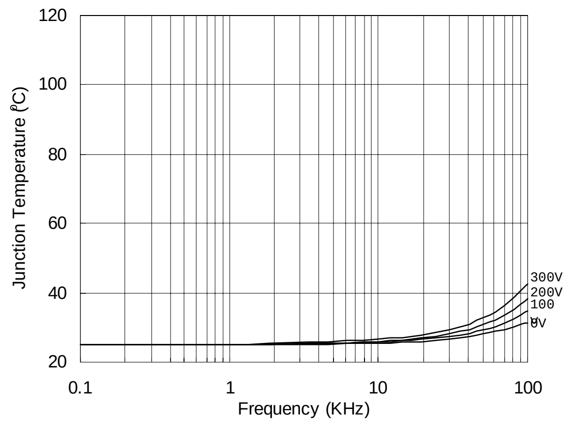


Figure 42. IR2136/IR21362/IR21363/IR21365 vs. Frequency (IRG4BC30W), R_{gate}=15Ω, V_{CC}=15V

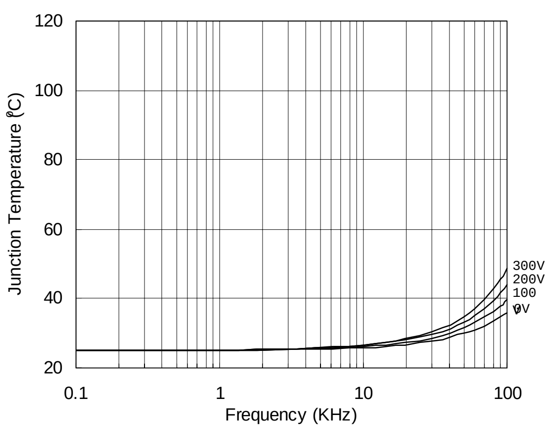


Figure 43. IR2136/IR21362/IR21363/IR21365 vs. Frequency (IRG4BC40W), R_{gate}=10Ω, V_{CC}=15V

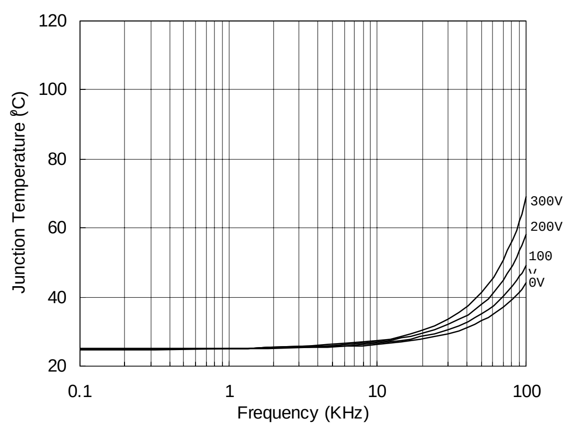


Figure 44. IR2136/IR21362/IR21363/IR21365 vs. Frequency (IRG4PC50W), R_{gate}=5Ω, V_{CC}=15V

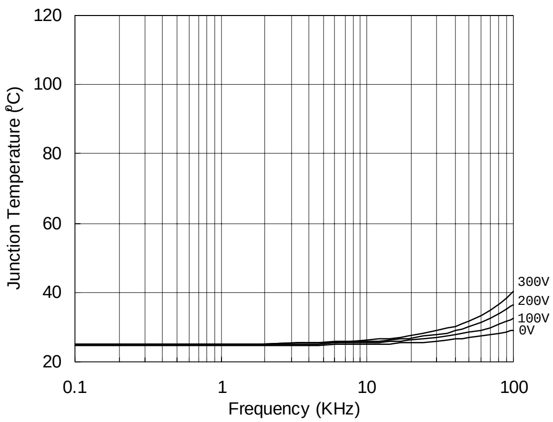


Figure 45. IR2136J/IR21362J/IR21363J/IR21365J vs. Frequency (IRG4BC20W), R_{gate}=33Ω, V_{CC}=15V

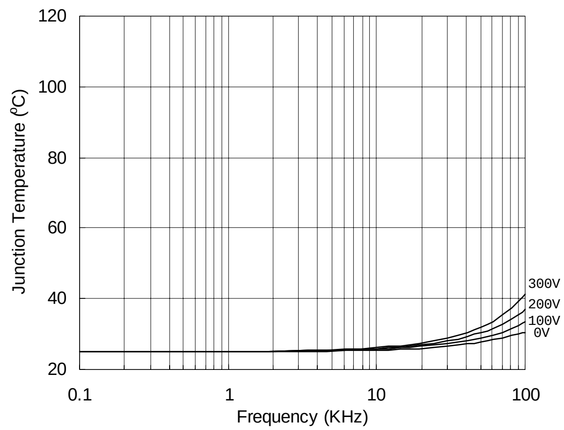


Figure 46. IR2136J/IR21362J/IR21363J/IR21365J vs. Frequency (IRG4BC30W), R_{gate}=15Ω, V_{CC}=15V

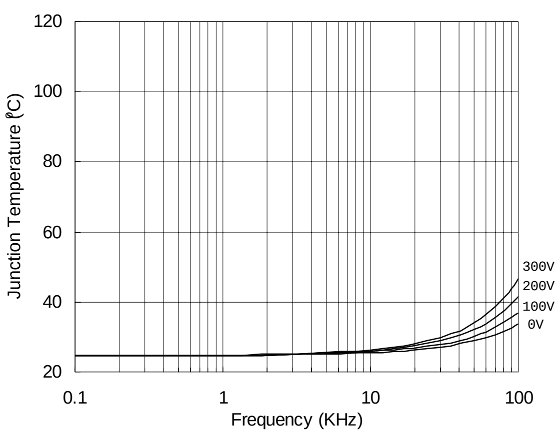


Figure 47. IR2136J/IR21362J/IR21363J/IR21365J vs. Frequency (IRG4BC40W), R_{gate}=10Ω, V_{CC}=15V

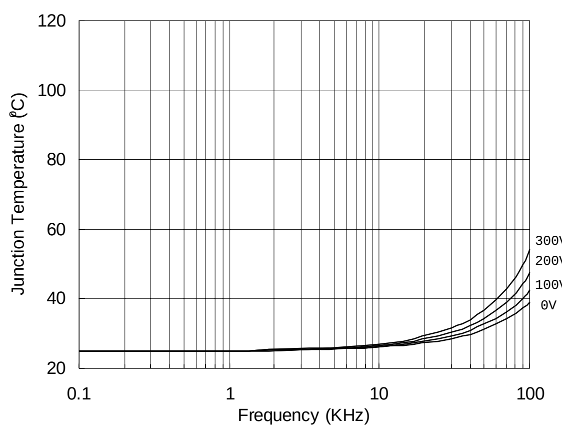


Figure 48. IR2136J/IR21362J/IR21363J/IR21365J vs. Frequency (IRG4PC50W), R_{gate}=5Ω, V_{CC}=15V

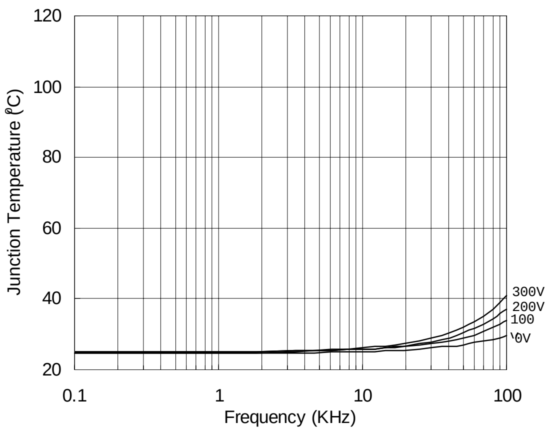


Figure 49. IR2136S/IR21362S/IR21363S/IR21365S vs. Frequency (IRG4BC20W), R_{gate}=33Ω , V_{CC}=15V

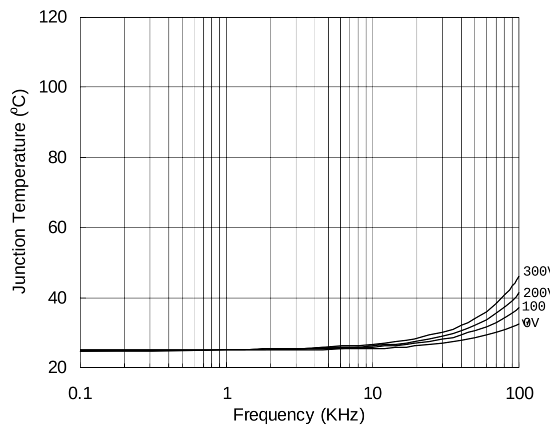


Figure 50. IR2136S/IR21362S/IR21363S/IR21365S vs. Frequency (IRG4BC30W), R_{gate}=15Ω , V_{CC}=15V

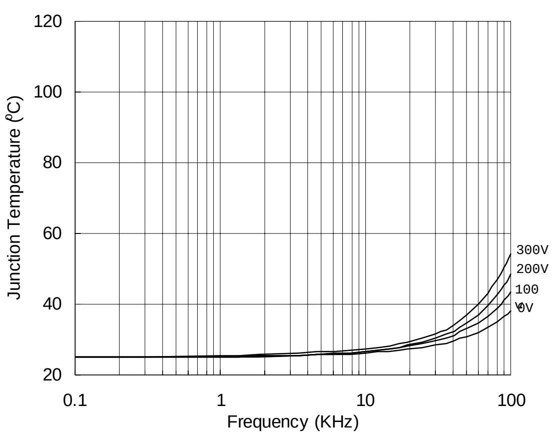


Figure 51. IR2136S/IR21362S/IR21363S/IR21365S vs. Frequency (IRG4BC40W), R_{gate}=10Ω , V_{CC}=15V

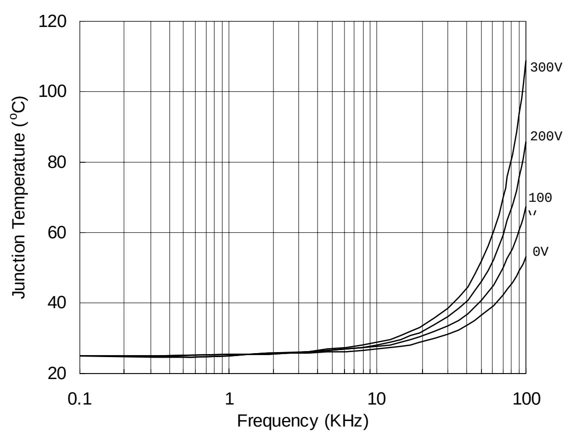
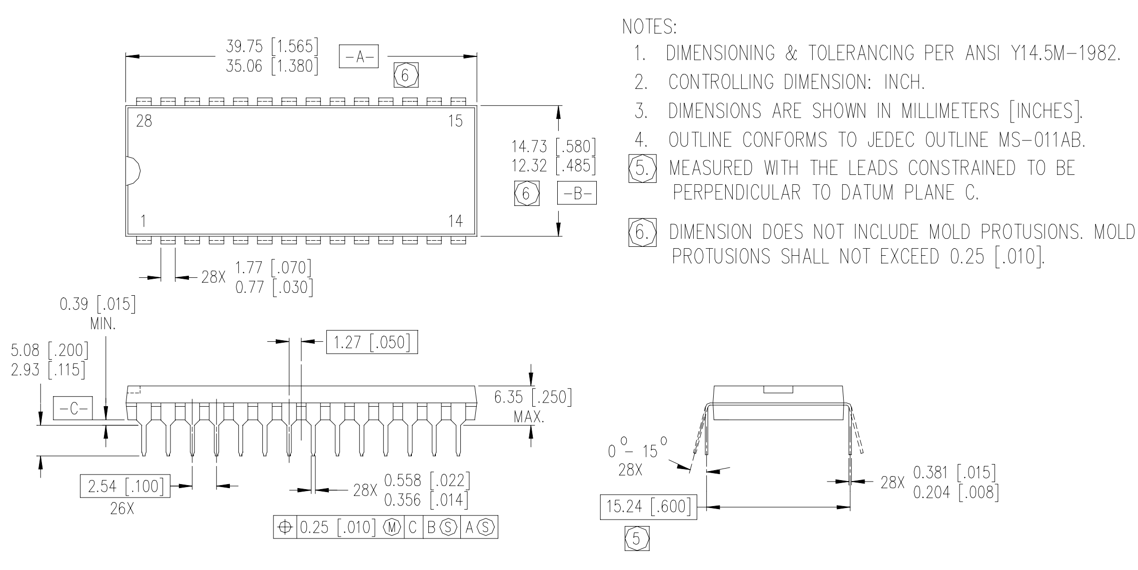


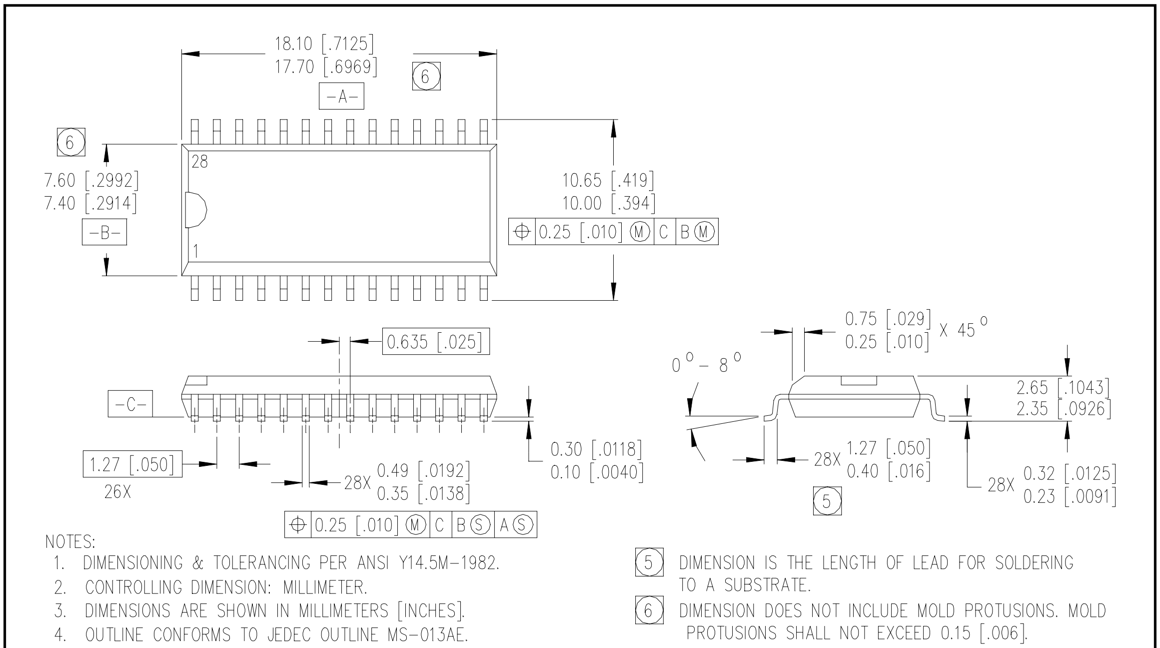
Figure 52. IR2136S/IR21362S/IR21363S/IR21365S vs. Frequency (IRG4PC50W), R_{gate}=5Ω , V_{CC}=15V

Case outlines



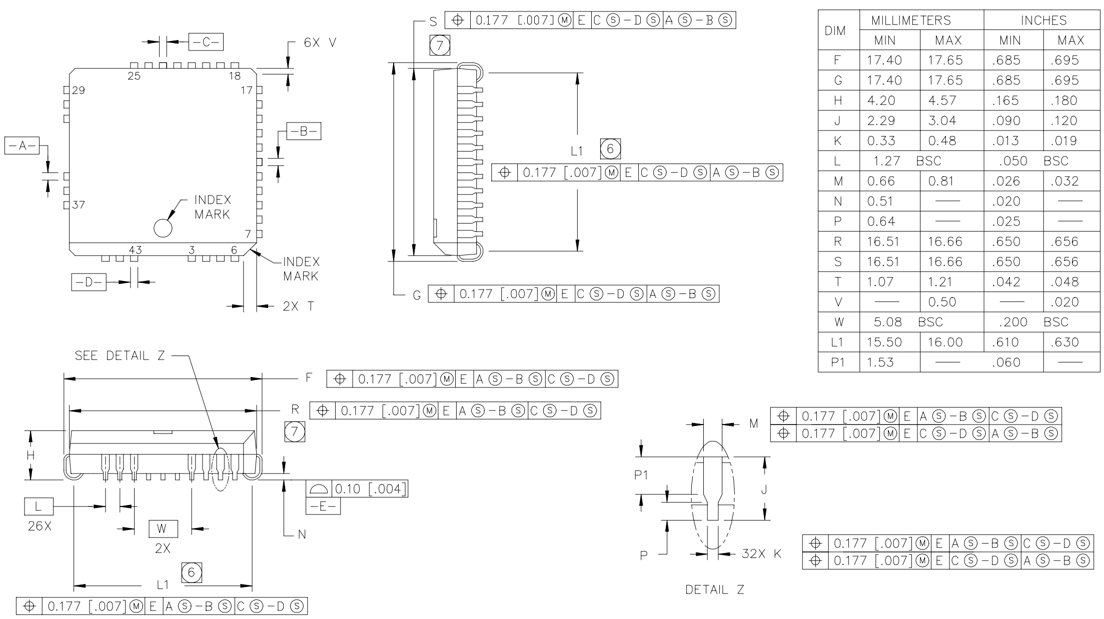
28-Lead PDIP (wide body)

01-6011
01-3024 02 (MS-011AB)



28-Lead SOIC (wide body)

01-6013
01-3040 02 (MS-013AE)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F	17.40	17.65	.685	.695
G	17.40	17.65	.685	.695
H	4.20	4.57	.165	.180
J	2.29	3.04	.090	.120
K	0.33	0.48	.013	.019
L	1.27 BSC		.050 BSC	
M	0.66	0.81	.026	.032
N	0.51	—	.020	—
P	0.64	—	.025	—
R	16.51	16.66	.650	.656
S	16.51	16.66	.650	.656
T	1.07	1.21	.042	.048
V	—	0.50	—	.020
W	5.08 BSC		.200 BSC	
L1	15.50	16.00	.610	.630
P1	1.53	—	.060	—

NOTES

1. DIMENSIONING & TOLERENCING PER ANSI Y14.5M-1982.
2. DIMENSIONS SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE MS-018AC.
5. DATUMS -A-, -B-, -C-, & -D- ARE DETERMINED BY WHERE THE TOP OF THE LEADS EXIT PLASTIC BODY AT MOLD PARTING LINE.
6. TO BE MEASURED AT -E- SEATING PLANE.
7. DIMENSIONS DO NOT INCLUDE MOLD FLASH, ALLOWABLE FLASH IS 0.254 [.010].

44-Lead PLCC w/o 12 leads

01-6009 00
01-3004 02(mod.) (MS-018AC)

International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas Street, El Segundo, California 90245 Tel: (310) 252-7105
http://www.irf.com/ Data and specifications subject to change without notice. 11/5/2002

NTP6N60, NTB6N60

Preferred Device

Advance Information

Power MOSFET 6 Amps, 600 Volts

N–Channel TO–220 and D²PAK

Designed for high voltage, high speed switching applications in power supplies, converters, power motor controls and bridge circuits.

Features

- Higher Current Rating
- Lower $R_{DS(on)}$
- Lower Capacitances
- Lower Total Gate Charge
- Tighter V_{SD} Specifications
- Avalanche Energy Specified

Typical Applications

- Switch Mode Power Supplies
- PWM Motor Controls
- Converters
- Bridge Circuits

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	600	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	600	Vdc
Gate–Source Voltage – Continuous – Non–Repetitive ($t_p \le$ 10 ms)	 V_{GS} V_{GSM}	 ± 20 ± 40	Vdc
Drain – Continuous – Continuous @ 100°C – Single Pulse ($t_p \le$ 10 μs)	 I_D I_D I_{DM}	 6.0 4.8 21	Adc
Total Power Dissipation Derate above 25°C	P_D	142 1.14	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Drain–to–Source Avalanche Energy – Starting T_J = 25°C (V_{DD} = 100 V, V_{GS} = 10 Vdc, I_L = 6 A, L = 25 mH, R_G = 25 Ω)	E_{AS}	450	mJ
Thermal Resistance – Junction–to–Case – Junction–to–Ambient – Junction–to–Ambient (Note 1.)	 $R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	 0.88 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

1. When surface mounted to an FR4 board using the minimum recommended pad size.

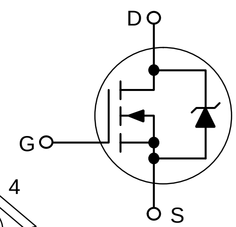
This document contains information on a new product. Specifications and information herein are subject to change without notice.

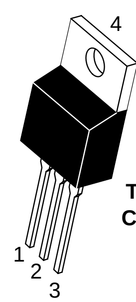
ON Semiconductor™

http://onsemi.com

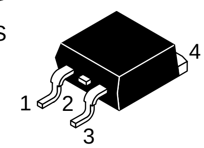
6 AMPERES
600 VOLTS
$R_{DS(on)}$ = 1200 mΩ

N–Channel



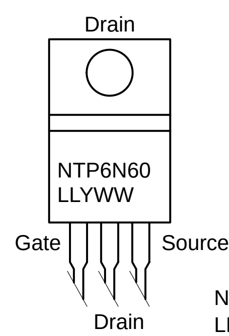


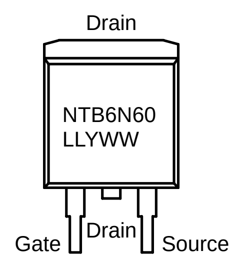
TO–220AB
CASE 221A
STYLE 5



D²PAK
CASE 418B
STYLE 2

MARKING DIAGRAMS AND PIN ASSIGNMENTS





NTx6N60	= Device Code
LL	= Location Code
Y	= Year
WW	= Work Week

ORDERING INFORMATION

Device	Package	Shipping
NTP6N60	TO–220AB	50 Units/Rail
NTB6N60	D²PAK	50 Units/Rail
NTB6N60T4	D²PAK	800/Tape & Reel

Preferred devices are recommended choices for future use and best overall value.

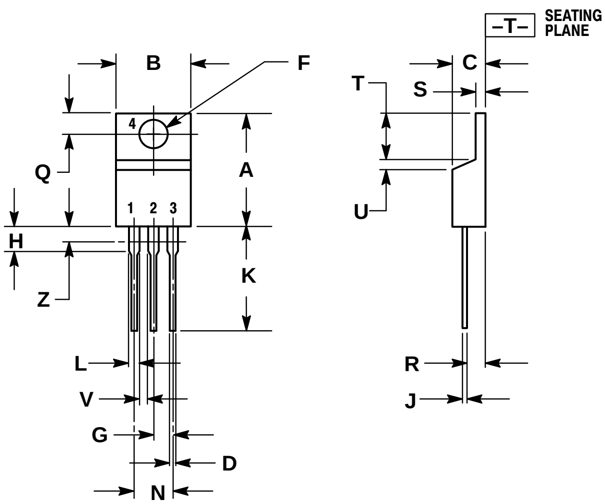
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	600	–	–	Vdc
Temperature Coefficient (Positive)			–	715	–	mV/°C
Zero Gate Voltage Collector Current (V_{DS} = 600 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	–	–	10	µAdc
(V_{DS} = 600 Vdc, V_{GS} = 0 Vdc, T_J =125°C)			–	–	100	
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		$I_{GSS(f)}$	–	–	100	nAdc
		$I_{GSS(r)}$	–	–	100	
ON CHARACTERISTICS (Note 2.)						
Gate Threshold Voltage I_D = 0.25 mA, V_{DS} = V_{GS}		$V_{GS(th)}$	2.0	2.6	4.0	Vdc
Temperature Coefficient (Negative)			–	6.6	–	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 3 Adc)		$R_{DS(on)}$	–	850	1200	mOhm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 6 Adc)		$V_{DS(on)}$	–	–	8.6	Vdc
(V_{GS} = 10 Vdc, I_D = 3 Adc, T_J = 125°C)			–	–	7.9	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 3 Adc)		g_{FS}	2.0	7.0	–	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	–	1190	1670	pF
Output Capacitance		C_{oss}	–	350	490	
Transfer Capacitance		C_{rss}	–	20	40	
SWITCHING CHARACTERISTICS (Note 3.)						
Turn–On Delay Time	(V_{DD} = 300 Vdc, I_D = 6 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	–	11	20	ns
Rise Time		t_r	–	10	20	
Turn–Off Delay Time		$t_{d(off)}$	–	34	70	
Fall Time		t_f	–	19	40	
Gate Charge	(V_{DS} = 480 Vdc, I_D = 6 Adc, V_{GS} = 10 Vdc)	Q_T	–	24	30	nC
		Q_1	–	6.0	–	
		Q_2	–	8.0	–	
		Q_3	–	12	–	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (Note 2.)	(I_S = 6 Adc, V_{GS} = 0 Vdc)	V_{SD}	–	0.85	1.0	Vdc
	(I_S = 6 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		–	0.73	–	
Reverse Recovery Time	(I_S = 6 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/µs)	t_{rr}	–	440	–	ns
		t_a	–	130	–	
		t_b	–	310	–	
Reverse Recovery Stored Charge		Q_{RR}	–	2.8	–	µC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die)		L_D	–	3.5	–	nH
(Measured from the drain lead 0.25″ from package to center of die)			–	4.5	–	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	–	7.5	–	

2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

PACKAGE DIMENSIONS

TO–220 THREE–LEAD
TO–220AB
CASE 221A–09
ISSUE AA

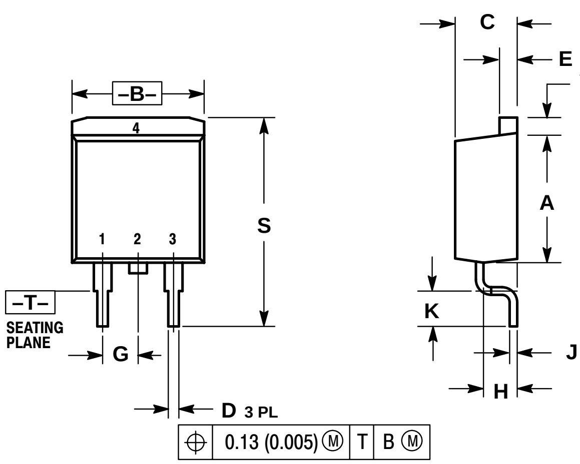


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

D2PAK
CASE 418B–03
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

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