# Apéndice B Hojas técnicas: LM555, Driver IR4427, IRFP450

## HOJAS TECNICAS

### LM555

National Semiconductor

February 2000

# LM555
# Timer

## General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits.

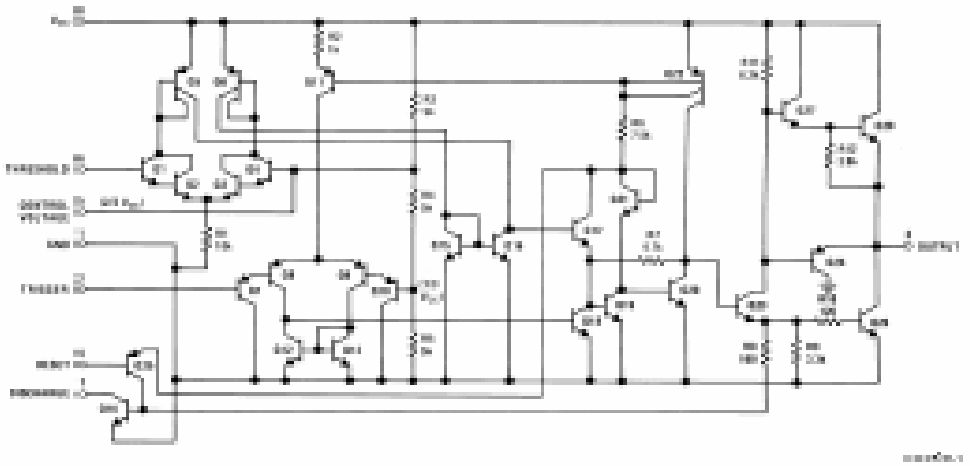
## Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output
- Available in 8-pin MSOP package

## Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

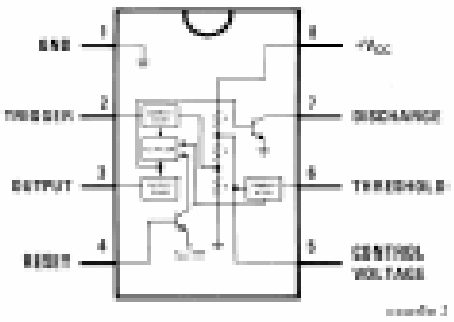
## Schematic Diagram



LM555

## Connection Diagram

**Dual-In-Line, Small Outline and Molded Mini Small Outline Packages**



**Top View**

## Ordering Information

| Package | Part Number | Package Marking | Media Transport | NSC Drawing |
|---|---|---|---|---|
| 8-Pin SOIC | LM555CM | LM555CM | Rails | M08A |
| | LM555CMX | LM555CM | 2.5k Units Tape and Reel | |
| 8-Pin MSOP | LM555CMM | Z55 | 1k Units Tape and Reel | MUA08A |
| | LM555CMMX | Z55 | 3.5k Units Tape and Reel | |
| 8-Pin MDIP | LM555CN | LM555CN | Rails | N08E |

International
IOR Rectifier

Data Sheet No. PD60177-D

# IR4426/IR4427/IR4428 (S)

## DUAL LOW SIDE DRIVER

### Features

* Gate drive supply range from 6 to 20V
* CMOS Schmitt-triggered inputs
* Matched propagation delay for both channels
* Outputs out of phase with inputs (IR4426)
* Outputs in phase with inputs (IR4427)
* OutputA out of phase with inputA and OutputB in phase with inputB (IR4428)

### Descriptions

The IR4426/IR4427/IR4428 (S) is a low voltage, high speed power MOSFET and IGBT driver. Proprietary latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays between two channels are matched.

### Product Summary

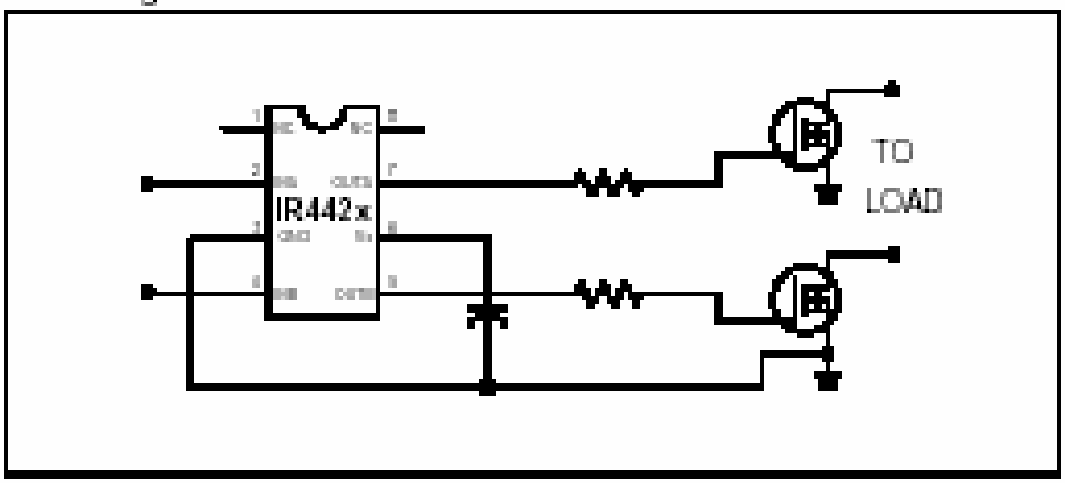
| | |
|---|---|
| Io+/- | 1.5A / 1.5A |
| VOUT | 6V - 20V |
| ton/off (typ.) | 85 & 85 ns |

### Packages

8 Lead PDIP

8 Lead SOIC

### Block Diagram



## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

| Symbol | Definition | | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_S$ | Fixed supply voltage | | -0.3 | 25 | V |
| $V_O$ | Output voltage | | -0.3 | $V_S$ + 0.3 | |
| $V_{IN}$ | Logic input voltage | | -0.3 | $V_S$ + 0.3 | |
| $P_D$ | Package power dissipation @ $T_A \leq +25°C$ | (8 Lead PDIP) | — | 1.0 | W |
| | | (8 lead SOIC) | — | 0.625 | |
| $Rth_{JA}$ | Thermal resistance, junction to ambient | (8 lead PDIP) | — | 125 | °C/W |
| | | (8 lead SOIC) | — | 200 | |
| $T_J$ | Junction temperature | | — | 150 | °C |
| $T_S$ | Storage temperature | | -55 | 150 | |
| $T_L$ | Lead temperature (soldering, 10 seconds) | | — | 300 | |

## Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to GND.

| Symbol | Definition | Min. | Max. | Units |
|---|---|---|---|---|
| $V_S$ | Fixed supply voltage | 6 | 20 | V |
| $V_O$ | Output voltage | 0 | $V_S$ | |
| $V_{IN}$ | Logic input voltage | 0 | $V_S$ | |
| $T_A$ | Ambient temperature | -40 | 125 | °C |

## DC Electrical Characteristics

$V_{BIAS}$ ($V_S$) = 15V, $T_A$ = 25°C unless otherwise specified. The $V_{IN}$, and $I_{IN}$ parameters are referenced to GND and are applicable to input leads: INA and INB. The $V_O$ and $I_O$ parameters are referenced to GND and are applicable to the output leads: OUTA and OUTB.

| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Logic "0" input voltage (OUTA=LO, OUTB=LO) (IR4426) Logic "1" input voltage (OUTA=HI, OUTB=HI) (IR4427) Logic "0" input voltage (OUTA=LO), Logic "1" input voltage (OUTB=HI) (IR4428) | 2.7 | — | — | V | |

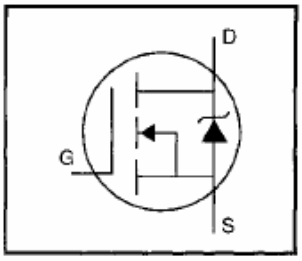
**International**
**IOR Rectifier**

PD-9.458C

# IRFP450

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements




$V_{DSS}$ = 500V

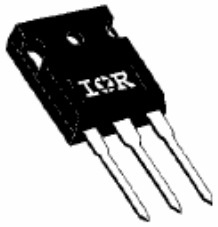
$R_{DS(on)}$ = 0.40Ω

$I_D$ = 14A

## Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247 package is preferred for commercial–industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole. It also provides greater creepage distance between pins to meet the requirements of most safety specifications.




TO-247AC

## Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10 V | 14 | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10 V | 8.7 | |
| $I_{DM}$ | Pulsed Drain Current ① | 56 | |
| $P_D$ @ $T_C$ = 25°C | Power Dissipation | 190 | W |
| | Linear Derating Factor | 1.5 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ±20 | V |
| $E_{AS}$ | Single Pulse Avalanche Energy ② | 760 | mJ |
| $I_{AR}$ | Avalanche Current ① | 8.7 | A |
| $E_{AR}$ | Repetitive Avalanche Energy ① | 19 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | 3.5 | V/ns |
| $T_J$<br>$T_{STG}$ | Operating Junction and<br>Storage Temperature Range | -55 to +150 | °C |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case) | |
| | Mounting Torque, 6-32 or M3 screw | 10 lbf•in (1.1 N•m) | |

## Thermal Resistance

| | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case | — | — | 0.65 | °C/W |
| $R_{\theta CS}$ | Case-to-Sink, Flat, Greased Surface | — | 0.24 | — | |
| $R_{\theta JA}$ | Junction-to-Ambient | — | — | 40 | |

# IRFP450

IOR

## Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 500 | — | — | V | $V_{GS}$=0V, $I_D$= 250µA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.63 | — | V/°C | Reference to 25°C, $I_D$= 1mA |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | — | 0.40 | Ω | $V_{GS}$=10V, $I_D$=8.4A ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | — | 4.0 | V | $V_{DS}$=$V_{GS}$, $I_D$= 250µA |
| $g_{fs}$ | Forward Transconductance | 9.3 | — | — | S | $V_{DS}$=50V, $I_D$=8.4A ④ |
| $I_{DSS}$ | Drain-to-Source Leakage Current | — | — | 25 | µA | $V_{DS}$=500V, $V_{GS}$=0V |
| | | — | — | 250 | | $V_{DS}$=400V, $V_{GS}$=0V, $T_J$=125°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS}$=20V |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS}$=-20V |
| $Q_g$ | Total Gate Charge | — | — | 150 | nC | $I_D$=14A |
| $Q_{gs}$ | Gate-to-Source Charge | — | — | 20 | | $V_{DS}$=400V |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | — | — | 80 | | $V_{GS}$=10V See Fig. 6 and 13 ④ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 17 | — | ns | $V_{DD}$=250V |
| $t_r$ | Rise Time | — | 47 | — | | $I_D$=14A |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 92 | — | | $R_G$=6.2Ω |
| $t_f$ | Fall Time | — | 44 | — | | $R_D$=17Ω See Figure 10 ④ |
| $L_D$ | Internal Drain Inductance | — | 5.0 | — | nH | Between lead, 6 mm (0.25in.) from package and center of die contact |
| $L_S$ | Internal Source Inductance | — | 13 | — | | |
| $C_{iss}$ | Input Capacitance | — | 2600 | — | pF | $V_{GS}$=0V |
| $C_{oss}$ | Output Capacitance | — | 720 | — | | $V_{DS}$= 25V |
| $C_{rss}$ | Reverse Transfer Capacitance | — | 340 | — | | f=1.0MHz See Figure 5 |

## Source-Drain Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | — | — | 14 | A | MOSFET symbol showing the integral reverse p-n junction diode. |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ③ | — | — | 56 | | |
| $V_{SD}$ | Diode Forward Voltage | — | — | 1.4 | V | $T_J$=25°C, $I_S$=14A, $V_{GS}$=0V ④ |
| $t_{rr}$ | Reverse Recovery Time | — | 540 | 810 | ns | $T_J$=25°C, $I_F$=14A |
| $Q_{RR}$ | Reverse Recovery Charge | — | 4.8 | 7.2 | µC | di/dt=100A/µs ④ |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is neglegible (turn-on is dominated by Ls+Ld) | | | | |