Apéndice B. Hoja de Especificaciones del Contador de década CD4017.

National Semiconductor

March 1988

CD4017BM/CD4017BC Decade Counter/Divider with 10 Decoded Outputs CD4022BM/CD4022BC Divide-by-8 Counter/Divider with 8 Decoded Outputs

General Description

The CD4017BM/CD4017BC is a 5-stage divide-by-10 Johnson counter with 10 decoded outputs and a carry out bit.

The CD4022BM/CD4022BC is a 4-stage divide-by-8 Johnson counter with 8 decoded outputs and a carry-out bit.

These counters are cleared to their zero count by a logical "1" on their reset line. These counters are advanced on the positive edge of the clock signal when the clock enable signal is in the logical "0" state.

The configuration of the CD4017BM/CD4017BC and CD4022BM/CD4022BC permits medium speed operation and assures a hazard free counting sequence. The 10/8 decoded outputs are normally in the logical "0" state and go to the logical "1" state only at their respective time slot. Each decoded output remains high for 1 full clock cycle. The carry-out signal completes a full cycle for every 10/8 clock input cycles and is used as a ripple carry signal to any succeeding stages.

Features

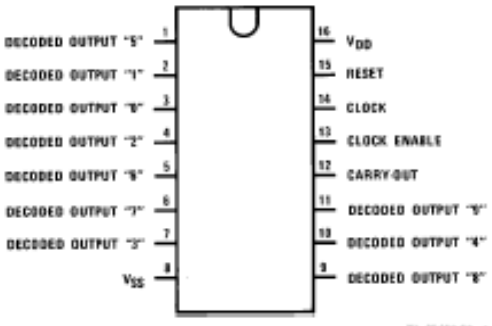
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	Fan out of 2 driving 74L or 1 driving 74LS
■ Medium speed operation	5.0 MHz (typ.) with 10V V_{DD}
■ Low power	10 μW (typ.)
■ Fully static operation	

Applications

- Automotive
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering

Connection Diagrams

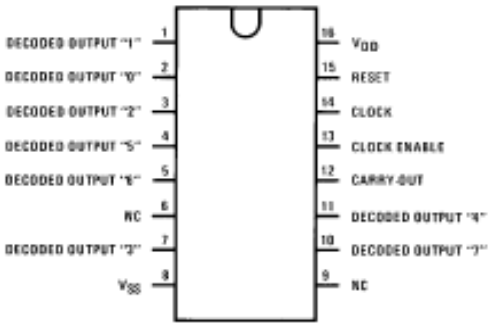
CD4017B
Dual-In-Line Package



TL/F/5950–1

Top View

CD4022B
Dual-In-Line Package



TL/F/5950–2

Top View

Order Number CD4017B or CD4022B

CD4017BM/CD4017BC Decade Counter/Divider with 10 Decoded Outputs
CD4022BM/CD4022BC Divide-by-8 Counter/Divider with 8 Decoded Outputs

..\DataSheets\CD4017.pdf

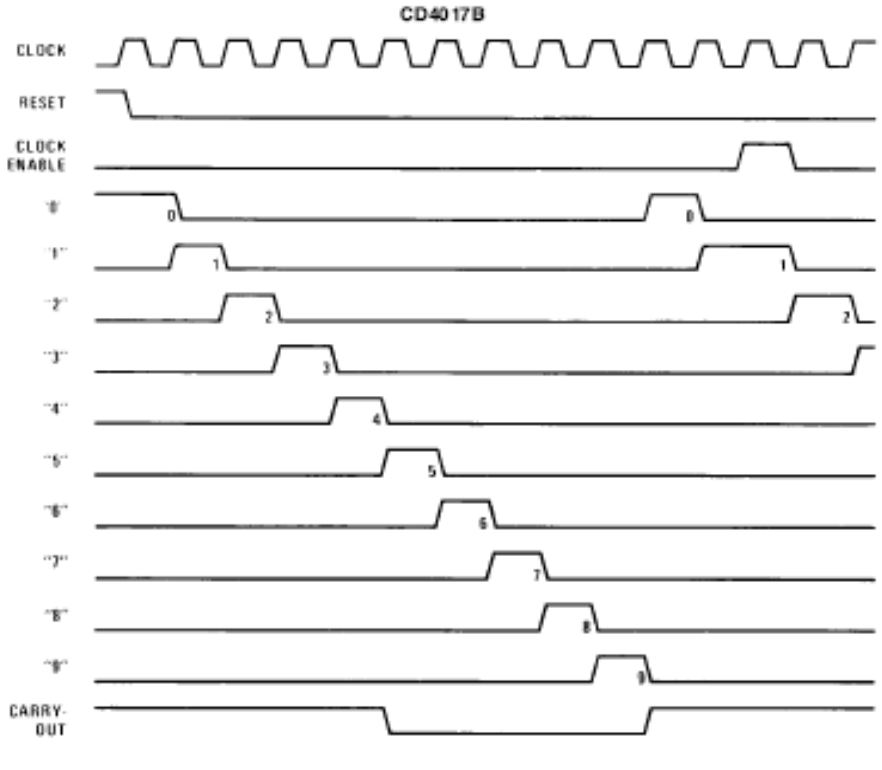
AC Electrical Characteristics*

T_A = 25°C, C_L = 50 pF, R_L = 200k, t_{rCL} and t_{fCL} = 20 ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RESET OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time Carry Out Line	V_{DD} = 5V		415	800	ns
		V_{DD} = 10V		160	320	ns
		V_{DD} = 15V		130	250	ns
	Carry Out Line	V_{DD} = 5V, C_L = 15 pF		240	480	ns
		V_{DD} = 10V, C_L = 15 pF		85	170	ns
		V_{DD} = 15V, C_L = 15 pF		70	140	ns
	Decode Out Lines	V_{DD} = 5V		500	1000	ns
		V_{DD} = 10V		200	400	ns
		V_{DD} = 15V		160	320	ns
t_W	Minimum Reset Pulse Width	V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		70	140	ns
		V_{DD} = 15V		55	110	ns
t_{REM}	Minimum Reset Removal Time	V_{DD} = 5V		75	150	ns
		V_{DD} = 10V		30	60	ns
		V_{DD} = 15V		25	50	ns

*AC Parameters are guaranteed by DC correlated testing.

Timing Diagrams



DataSheets\CD4017.pdf