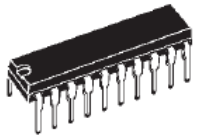
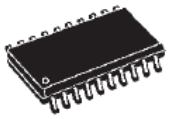
L297

STEPPER MOTOR CONTROLLERS

- NORMAL/WAVE DRIVE
- HALF/FULL STEP MODES
- CLOCKWISE/ANTICLOCKWISE DIRECTION
- SWITCHMODE LOAD CURRENT REGULATION
- PROGRAMMABLE LOAD CURRENT
- FEW EXTERNAL COMPONENTS
- RESET INPUT & HOME OUTPUT
- ENABLE INPUT



DIP20



SO20

ORDERING NUMBERS : L297/1 (DIP20)
L297D (SO20)

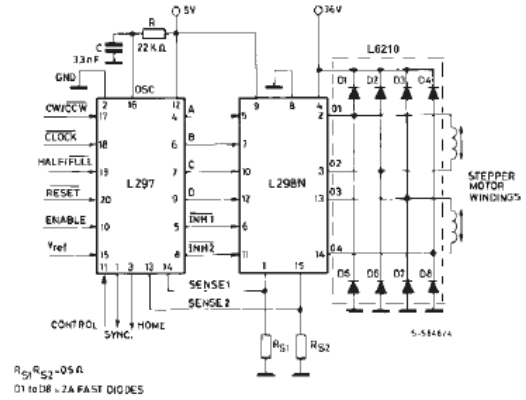
DESCRIPTION

The L297 Stepper Motor Controller IC generates four phase drive signals for two phase bipolar and four phase unipolar step motors in microcomputer-controlled applications. The motor can be driven in half step, normal and wawe drive modes and on-chip PWM chopper circuits permit switch-mode control of the current in the windings. A feature of this device is that it requires only clock, direction and mode input signals. Since the phase are generated internally the burden on the microprocessor, and the programmer, is greatly reduced. Mounted in DIP20 and SO20 packages, the L297 can be used with monolithic bridge drives such as the L298N or L293E, or with discrete transistors and darlingtons.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply voltage	10	V
V_i	Input signals	7	V
P_{tot}	Total power dissipation (T_{amb} = 70°C)	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to + 150	°C

TWO PHASE BIPOLAR STEPPER MOTOR CONTROL CIRCUIT



ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test conditions	Min.	Typ	Max.	Unit
I_{leak}	Leakage current (pin 3)	V_{CE} = 7 V			1	µA
V_{sat}	Saturation voltage (pin 3)	I = 5 mA			0.4	V
V_{off}	Comparators offset voltage (pins 13, 14, 15)	V_{ref} = 1 V			5	mV
I_o	Comparator bias current (pins 13, 14, 15)		-100		10	µA
V_{ref}	Input reference voltage (pin 15)		0		3	V
t_{CLK}	Clock time		0.5			µs
t_S	Set up time		1			µs
t_H	Hold time		4			µs
t_R	Reset time		1			µs
t_{RCLK}	Reset to clock delay		1			µs

INTEGRATED CIRCUITS
UNITRODE

L293
L293D

Push-Pull Four Channel Driver

FEATURES

- Output Current 1A Per Channel (600mA for L293D)
- Peak Output Current 2A Per Channel (1.2A for L293D)
- Inhibit Facility
- High Noise Immunity
- Separate Logic Supply
- Over-Temperature Protection

DESCRIPTION

The L293 and L293D are quad push-pull drivers capable of delivering output currents to 1A or 600mA per channel respectively. Each channel is controlled by a TTL-compatible logic input and each pair of drivers (a full bridge) is equipped with an inhibit input which turns off all four transistors. A separate supply input is provided for the logic so that it may be run off a lower voltage to reduce dissipation.

Additionally the L293D includes the output clamping diodes within the IC for complete interfacing with inductive loads.

Both devices are available in 16-pin Batwing DIP packages. They are also available in Power S0IC and Hermetic DIL packages.

TRUTH TABLE

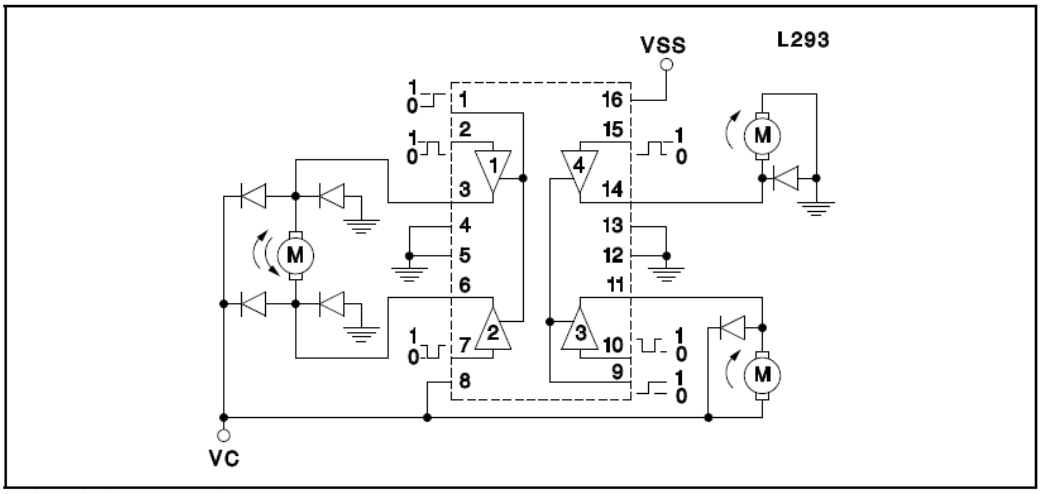
V_I (each channel)	V_{INH}*	V_O
H	H	H
L	H	L
H	L	X**
L	L	X**

**Relative to the considered channel*
***High output impedence*

ABSOLUTE MAXIMUM RATINGS

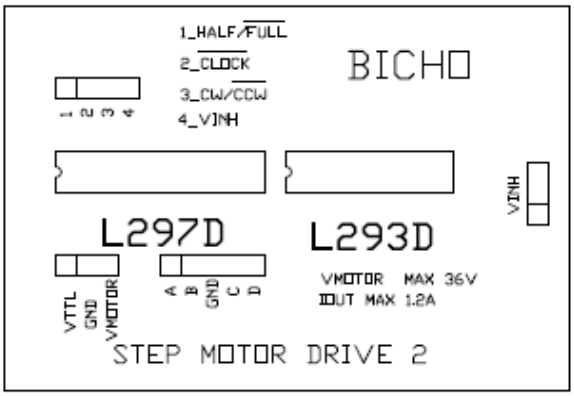
Collector Supply Voltage, V_C 36V
Logic Supply Voltage, V_{SS} 36V
Input Voltage, V_I 7V
Inhibit Voltage, V_{INH} 7V
Peak Output Current (Non-Repetitive), I_{OUT} (L293) 2A
I_{OUT} (L293D) 1.2A
Total Power Dissipation
at Tground-pins = 80°C, N Batwing pkg, (Note) 5W
Storage and Junction Temperature, Tstg, T_J . . . . . -40 to +150°C
Note:Consult packaging section of Databook for thermal limitations and considerations of packages.

BLOCK DIAGRAM

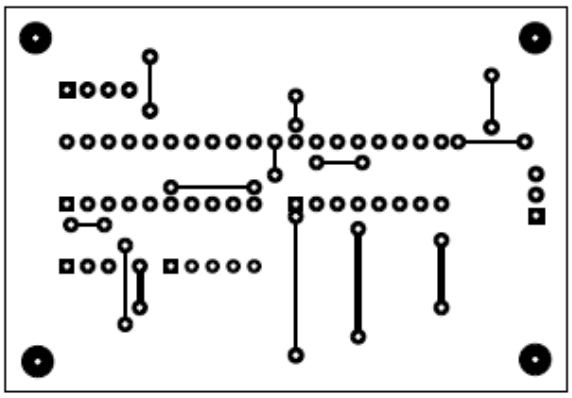


Note: Output diodes are internal in L293D.

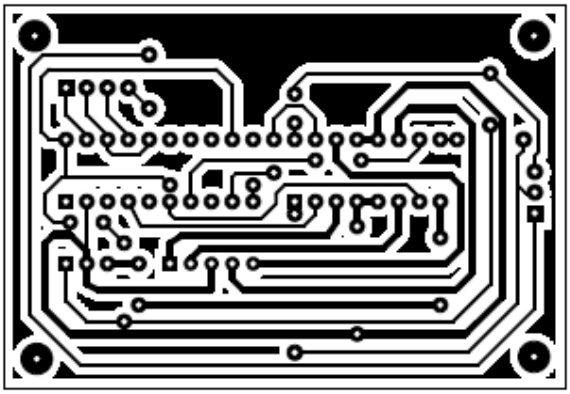
Tarjeta de circuito impreso del controlador de motor a pasos



Rotulado del controlador de motor a pasos



Capa superior de controlador de motor a pasos

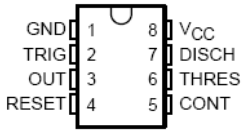


Capa inferior de controlador de motor a pasos

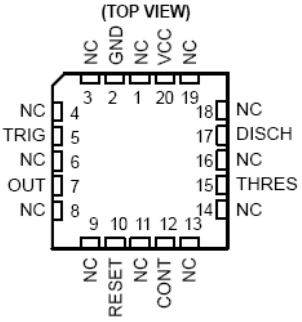
SLFS022C – SEPTEMBER 1973 – REVISED FEBRUARY 2002

- **Timing From Microseconds to Hours**
- **Astable or Monostable Operation**
- **Adjustable Duty Cycle**
- **TTL-Compatible Output Can Sink or Source up to 200 mA**
- **Designed To Be Interchangeable With Signetics NE555, SA555, and SE555**

NE555 . . . D, P, PS, OR PW PACKAGE
SA555 . . . D OR P PACKAGE
SE555 . . . D, JG, OR P PACKAGE
(TOP VIEW)



SE555 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices are precision timing circuits capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor.

The threshold and trigger levels normally are two-thirds and one-third, respectively, of V_{CC}. These levels can be altered by use of the control-voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset (RESET) input can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset and the output goes low. When the output is low, a low-impedance path is provided between discharge (DISCH) and ground.

The output circuit is capable of sinking or sourcing current up to 200 mA. Operation is specified for supplies of 5 V to 15 V. With a 5-V supply, output levels are compatible with TTL inputs.

The NE555 is characterized for operation from 0°C to 70°C. The SA555 is characterized for operation from –40°C to 85°C. The SE555 is characterized for operation over the full military range of –55°C to 125°C.

AVAILABLE OPTIONS

T_A	PACKAGE					
	V_{THRES} MAX V_{CC} = 15 V	SMALL OUTLINE (D, PS)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	PLASTIC THIN SHRINK SMALL OUTLINE (PW)
0°C to 70°C	11.2 V	NE555D NE555PS	—	—	NE555P	NE555PW
–40°C to 85°C	11.2 V	SA555D	—	—	SA555P	—
–55°C to 125°C	10.6 V	SE555D	SE555FK	SE555JG	SE555P	—

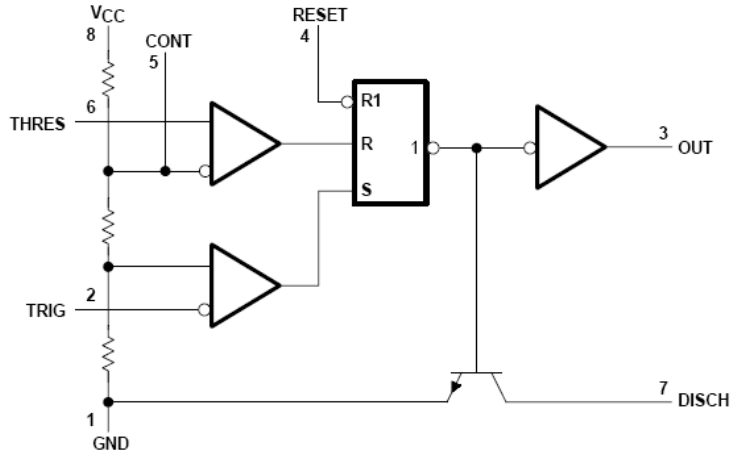
The D package is available taped and reeled. Add the suffix R to the device type (e.g., NE555DR). The PS and PW packages are only available taped and reeled.

FUNCTION TABLE

RESET	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	<1/3 V_{DD}	Irrelevant	High	Off
High	>1/3 V_{DD}	>2/3 V_{DD}	Low	On
High	>1/3 V_{DD}	<2/3 V_{DD}	As previously established	

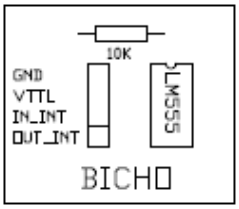
† Voltage levels shown are nominal.

functional block diagram

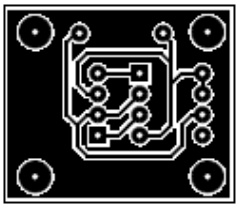


Pin numbers shown are for the D, JG, P, PS, and PW packages.
NOTE A: RESET can override TRIG, which can override THRES.

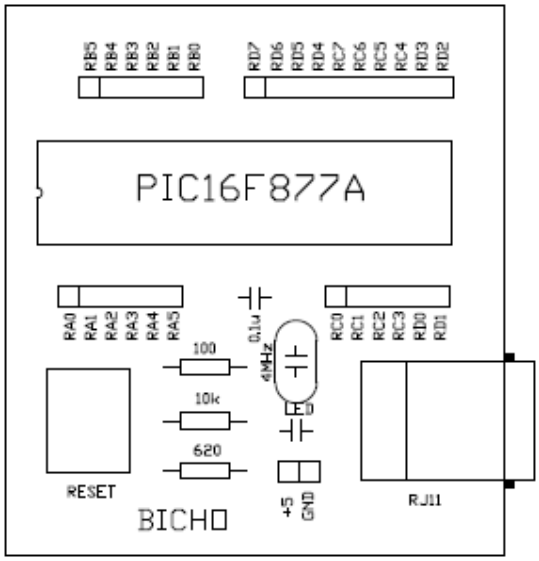
Tarjeta de circuito impreso del circuito antirrebotes



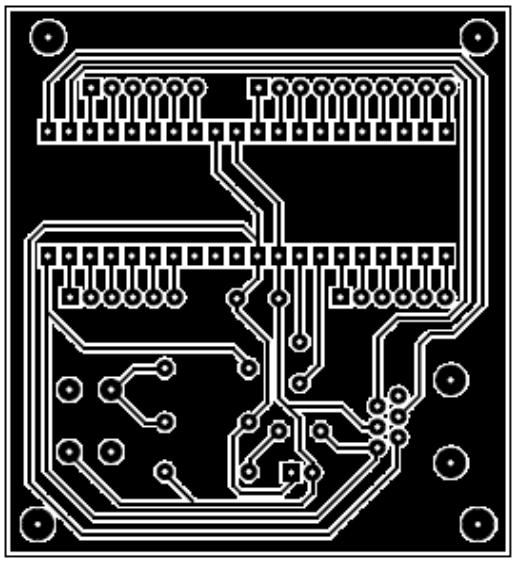
Rotulado del circuito antirrebotes


Capa inferior del circuito antirrebotes

Tarjeta de circuito impreso de la tarjeta de monitoreo y calibración

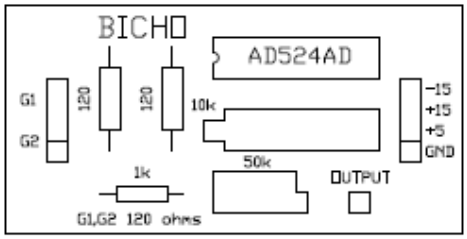


Rotulado de la tarjeta de monitoreo y calibración

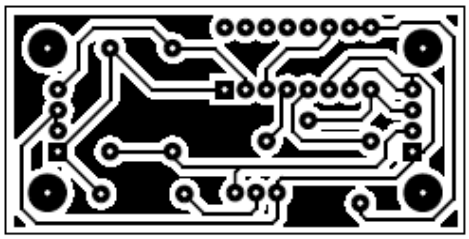


Capa inferior de la tarjeta de monitoreo y calibración

Tarjeta de circuito impreso de la tarjeta de acondicionamiento de la galga

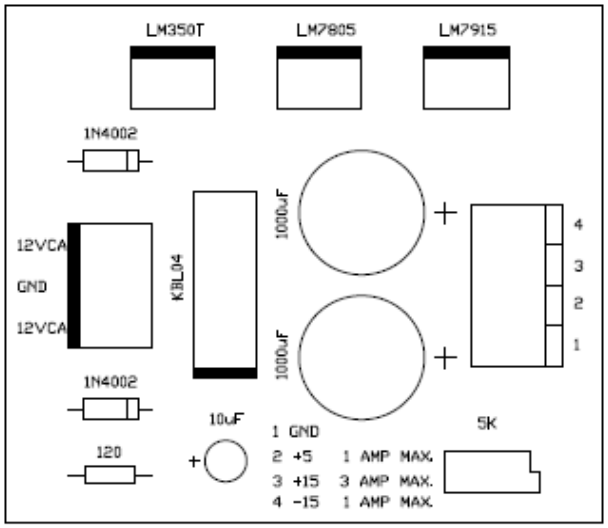


Rotulado de la tarjeta de acondicionamiento de la galga

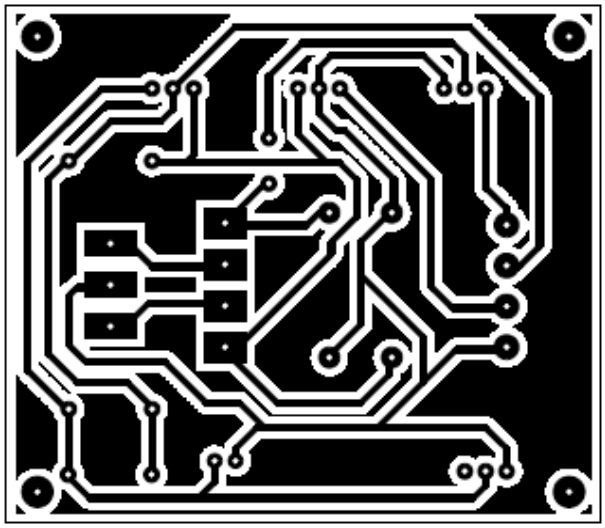


Capa inferior de la tarjeta de acondicionamiento de la galga

Tarjeta de circuito impreso de la fuente de alimentación

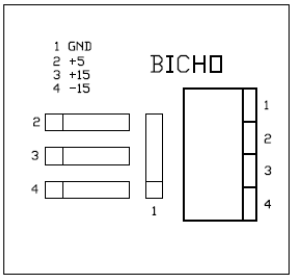


Rotulado de la fuente de alimentación.

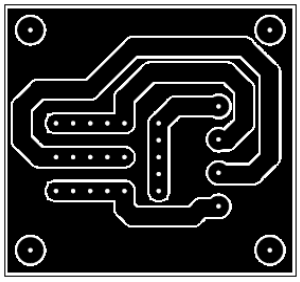


Capa inferior de la fuente de alimentación

Tarjeta de circuito impreso del centro de carga



Rotulado del centro de carga



Capa inferior del centro de carga